MODEL DQ214
DISC CONTROLLER
INSTRUCTION MANUAL

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LOGIC CORP.
DILOG

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DISC CONTROLLER
INSTRUCTION MANUAL

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DISTRIBUTED LOGIC CORP. DILOG

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DESCRIPTION

INTRODUCTION

This manual describes the installation, operation, programming, troubleshooting, and theory of operation of Distributed Logic Corporation (DILOG) Model DQ214 Disc Controller. The controller interfaces DEC* LSI-11 based computer systems to one or two SMD I/O disc drives, including 8- and 14-inch Winchester, SMD pack and CMD cartridge type drives. The complete controller occupies one quad module in the backplane. Full sector buffering in the controller matches the transfer rate of the disc drive and the CPU. The controller is compatible with RL01/RL02 software drivers in RT-11, RSX-11 and RSTS.

CONTROLLER CHARACTERISTICS

The disc controller links the LSI-11 computer to one or two disc storage units. Commands from the computer are received and interpreted by the controller and translated into a form compatible with the disc units. Buffering and signal timing for data transfers between the computer and the discs are performed by the controller.

*DEC, RSX and RSTS are registered trademarks of Digital Equipment Corporation.

A microprocessor is the sequence and timing center of the controller. The control information is stored as firmware instructions in Read Only Memory (ROM) on the controller board. One section of the ROM contains a diagnostic program that tests the functional operation of the controller. This self test is performed automatically each time power is applied. A green diagnostic LED on the controller board lights if self test passes.

Data transfers are directly to and from the computer memory using the DMA facility of the LSI-11 I/O bus. In addition, the controller monitors the status of the disc units and the data being transferred and presents this information to the computer upon request. An error correction code with a 56-bit checkword corrects error bursts up to 11 bits. To compensate for media errors, bad sectors are skipped and alternates assigned, and there is an automatic retry feature for read errors. The controller is capable of addressing four megabytes and controlling up to two disc drives in various configurations up to a total on-line formatted capacity of 41.94 megabytes. Figure 1-1 is a simplified diagram of a disc system illustrating the interfaces of the controller.

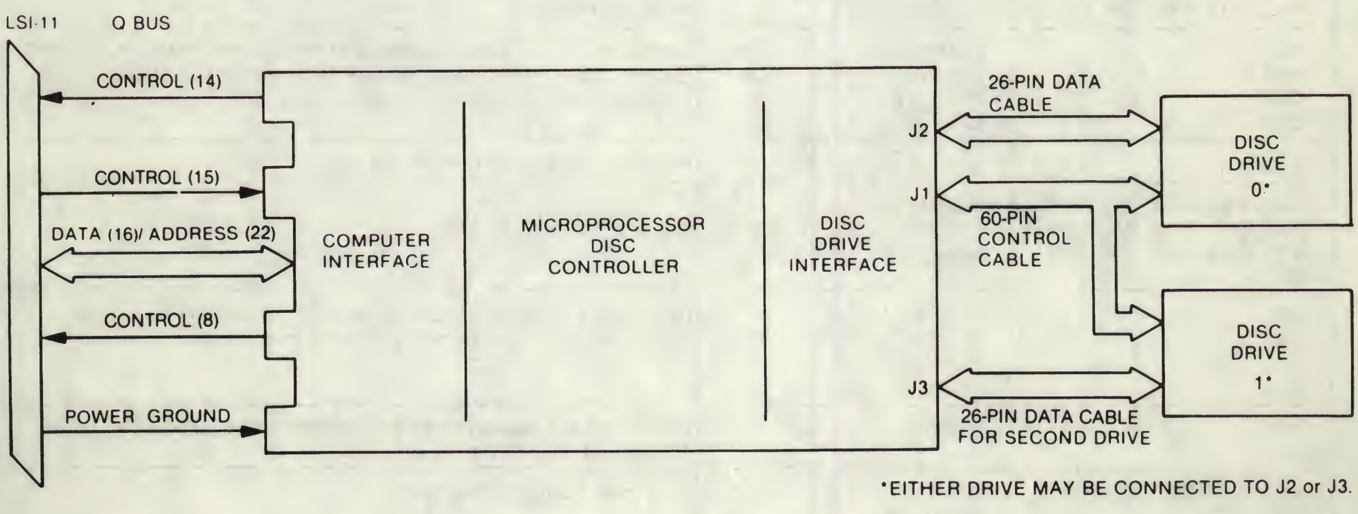


Figure 1-1. Disc Controller System Simplified Diagram

LSI-11 Q BUS INTERFACE

Commands, data and status transfers between the controller and the computer are executed via the parallel I/O bus (Q bus) of the computer. Data transfers are direct to memory via the DMA facility of the Q bus; commands and status are under programmed I/O. Controller/Q-bus interface lines are listed in Table 1-1.

Table 1-1. Controller/Q-Bus Interface Lines

Bus Pin	Mnemonic	Controller Input/ Output	Description
AC2, AJ1, AM1, AT1, BJ1, BM1, BT1, BC2, CC2, CJ1, CM1, CT1, DC2, DJ1, DM1, DT1	GND	O	Signal Ground and DC return.
AN1	BDMR L	O	Direct Memory Access (DMA) request from controller: active low.
AP1	BHALT L	N/A	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREF L	N/A	Memory Refresh.
BA1	BDCOK H	I	DC power OK. All DC voltages are normal.
BB1	BPOK H	N/A	Primary power OK. When low activates power fail trap sequence.
BN1	BSACK L	O	Select Acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	O	External Event Interrupt Request. Real Time Clock Control.
AA2, BA2, BV1, CA2, DA2	+5	I	+5 volt system power.
AD2, BD2	+12	N/A	+12 volt system power.
AE2	BDOUT L	I/O	Data Out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	I/O	Reply from slave to BDOUT or BDIN and during IAK.
AH2	BDIN L	I/O	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNC L	I/O	Synchronize: becomes active when master places address on bus; stays active during transfer.
AK2	BWTBT L	I/O	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AL2, AA1, AB1, BP1	BIRQ4L,5,6,7	O	Interrupt Request.
AM2 AN2 CM2 CN2	BIAK1I L BIAK1O L BIAK2I L BIAK2O L	I O I O	Serial Interrupt Acknowledge input and output lines routed from Q bus, through devices, and back to processor to establish an interrupt priority chain.
AT2	BINIT L	I	Initialize. Clears devices on I/O bus.
AU2, AV2, BE2, BF2, BH2, BJ2, BK2, BL2, BM2, BN2, BP2, BR2, BS2, BT2, BU2, BV2	BDAL0 L through BDAL15 L	I/O	Data/Address lines, 0-15
AR2 AS2 CR2 CS2	BDMG1I L BDMG1O L BDMG2I L BDMG2O L	I O I O	DMA Grant Input and Output. Serial DMA priority line from computer, through devices and back to computer.
AP2	BBS7 L	I	Bank 7 Select. Asserted by bus master when address in upper 4K bank is placed on the bus.
AC1, AD1, BC1, BD1, BE1, BF1	BDAL 16 L -BDAL 21 L	O	Extended Address Bits 16-21

INTERRUPT

The interrupt vector address is factory set to address 160. The vector address is programmed in a PROM on the controller, allowing user selection.

Interrupt requests are generated under the following conditions:

1. When the Controller Ready bit is set upon completion of a command.
2. When any drive sets an associated Attention Flag in the Attention register and the Controller Ready bit is set.
3. When the controller or any drive indicates the presence of an error by setting the combined Error/Reset bit in the Control and Status register.
4. A forced interrupt may be generated by the Controller Ready and Interrupt Enable bits.

DISC INTERFACE

The controller interfaces one or two disc drives through 60- and 26-pin cables. If two drives are used, the 60-pin control cable ("A" cable) is daisy chained to drive 0 and 1. The 26-pin cables ("B" cable) are connected separately from the controller to each drive. The maximum length of the 60-pin cable is 100 feet. The maximum length of the 26-pin cable is 50 feet. Table 1-2 lists the 60-pin interface signals, and Table 1-3 lists the 26-pin interface signals. Either 26-pin connector may be connected to either Drive 0 or Drive 1.

OPERATING SYSTEM COMPATIBILITY

RT-11: The emulation is transparent to the RT-11 version 4.0 operating system, using the standard device handler supplied by DEC.

RSX-11: The emulation is transparent to the RXS-11 version 4.0 operating system, using the standard device handler supplied by DEC.

RSTS: The emulation is transparent to the RSTS version 7.2 operating system, using the standard device handler supplied by DEC.

Table 1-2. Controller To Drive I/O Interface—"A" Cable

Signal Name (DILOG Term)	Pin Polarity (Active) –	+	Source
DEVICE SELECT 0 (USEL0)	23	53	Controller
DEVICE SELECT 1 (USEL1)	24	54	Controller
DEVICE SELECT 2 (USEL2)	26	56	Controller
DEVICE SELECT 3 (USEL3)	27	57	Controller
SELECT ENABLE (USTAG)	22	52	Controller
SET CYLINDER TAG (TAG1)	1	31	Controller
SET HEAD TAG (TAG2)	2	32	Controller
CONTROL SELECT (TAG3)	3	33	Controller
BUS OUT 0 (BIT0)	4	34	Controller
BUS OUT 1 (BIT1)	5	35	Controller
BUS OUT 2 (BIT2)	6	36	Controller
BUS OUT 3 (BIT3)	7	37	Controller
BUS OUT 4 (BIT4)	8	38	Controller
BUS OUT 5 (BIT5)	9	39	Controller
BUS OUT 6 (BIT6)	10	40	Controller
BUS OUT 7 (BIT7)	11	41	Controller
BUS OUT 8 (BIT8)	12	42	Controller
BUS OUT 9 (BIT9)	13	43	Controller
BUS OUT 10 (BIT10)	30	60	Controller
DEVICE ENABLE (OCD)	14	44	Controller
INDEX (INDEX)	18	48	Drive
SECTOR MARK (SEC)	25	55	Drive
FAULT (FAULT)	15	45	Drive
SEEK ERROR (SERR)	16	46	Drive
ON CYLINDER (ONCYL)	17	47	Drive
UNIT READY (UNRDY)	19	49	Drive
WRITE PROTECTED (WPRT)	28	58	Drive
ADDRESS MARK (AMF)	20	50	Drive
BUS-DUAL-PORT ONLY	21	51	Drive
SEQUENCE IN (PICK)	29		Controller
HOLD (HOLD)	59		Controller

Table 1-3. Controller To Drive I/O Interface—"B" Cable

Signal (DILOG Term)	Pin Polarity (Active) –	+	Ground	Source
Ground			1	
Servo Clock (SCLOCK)	2	14		Drive
Ground			15	
Read Data (RDATA)	3	16		Drive
Ground			4	
Read Clock (RCLOCK)	17	5		Drive
Ground			18	
Write Clock (WCLOCK)	6	19		Controller
Ground			7	
Write Data (WDATA)	8	20		Controller
Ground			21	
Unit Selected (USEL)	22	9		Drive
Seek End (SEEK)	10	23		Drive
Ground			11	
Reserved for Index	12	24		
Ground			25	
Reserved for Sector	13	26		

CONTROLLER SPECIFICATIONS*

Mechanical—The Model DQ214 is completely contained on one quad module 10.44 inches wide by 8.88 inches deep and plugs into and requires one slot in any DEC Q-Bus based backplane.

Computer I/O

Register Address (PROM selectable)
—Control Status (RLCS) 774 400
—Current Bus Address (RLBA) 774 402
—Disc Address (RLDA) 774 404
—Multipurpose (RLMP) 774 406
—Address Extension (RLBAE) 774 410

Data Transfer
—Method: DMA
—Maximum block size transferred in a single operation is 20K bytes.

Bus Load
—1 std unit load

Address Ranges
—Disc drive: up to 50 megabytes total
—Computer memory: to 4 megabytes

Interrupt Vector Address
—PROM selectable (factory set at 160, priority level BR5)

Disc Drive I/O

Connector—One 60-pin type "A" flat ribbon cable connector mounted on outer edge of controller module. Two 26-pin type "B" ribbon cables (1 for each drive interfaced with).

Signal—SMD A/B flat cable compatible.

Power—+5 volts at 3.5 amps, +12 volts at 300 milliamps from computer power supply.

Environment—Operating temperature 40°F to 140°F, humidity 10 to 95% non-condensing.

Shipping Weight—5 pounds, includes documentation and cables.

*Specifications subject to change without notice.

SECTION 2
INSTALLATION

INSPECTION

The padded shipping carton that contains the controller board also contains an instruction manual and cables to the first disc drive if this option is exercised. The controller is completely contained on one quad-module printed circuit board. Disc drives, if supplied, are contained in separate shipping cartons. Inspect the controller and cables for damage.

CAUTION

If damage to any of the components is noted, do not install. Immediately inform the carrier and DILOG.

Installation instructions for the disc drive(s) are contained in the disc drive manual. Before installing any components of the disc system, read Sections 1, 2 and 3 of this manual. Figure 2-1 illustrates the configuration of the controller. Tables 2-1 and 2-2 describe switch and jumper settings.

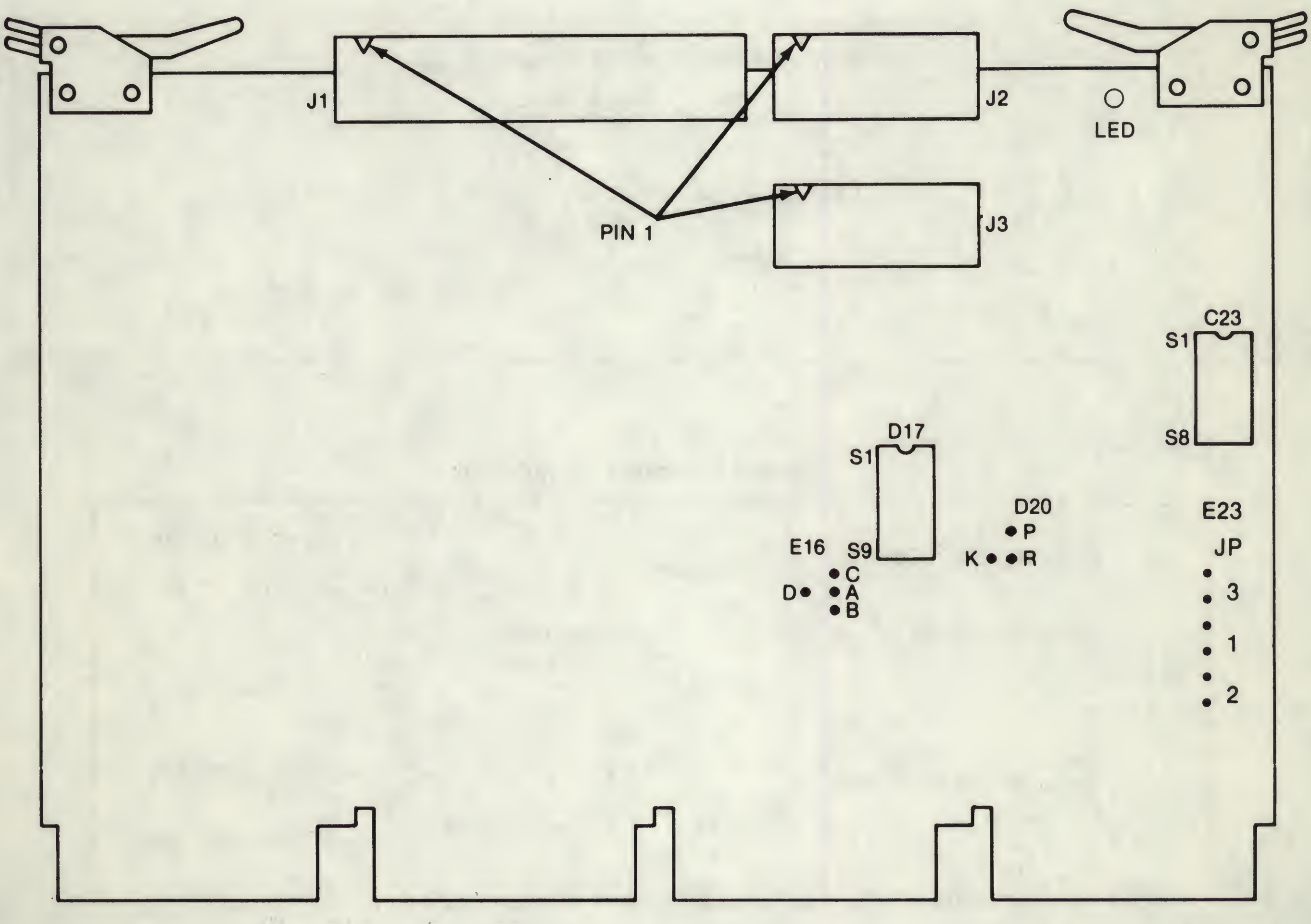


Figure 2-1. Controller Configuration

Table 2-1. Configuration Switches

LOCATION D17 SWITCHES

$\underbrace{\text{S1 (LSB)} \quad \text{S2} \quad \text{S3 (MSB)}}$
Binary Number of the first logical unit of the second physical drive.*

S4
ON = Bootstrap enable
OFF = Bootstrap disable

S5
ON = Controller error correction
OFF = CPU error correction

$\underbrace{\text{S6 (LSB} \quad \text{S7} \quad \text{S8 (MSB)}}$
Binary number of last addressable logical unit.

*For example, if there are four logical units (numbered 0-3) in the first drive, set the switches for the fifth logical unit (number 4) as follows:

(LSB) S1	S2	(MSB) S3
0	0	1

Note

If S1, S2, and S3 are off (000), the controller will default to all logical units on the first physical drive (drive 0). Because of the characteristics of some operating systems, the switches should be set for two drives even if only one drive is present.

LOCATION C23 SWITCHES

Switch	Position	Logical Unit and Emulation
S1	ON	LU0 = RL02
	OFF	LU0 = RL01
S2	ON	LU1 = RL02
	OFF	LU1 = RL01
S3	ON	LU2 = RL02
	OFF	LU2 = RL01
S4	ON	LU3 = RL02
	OFF	LU3 = RL01
S5-S8 NOT USED		

Table 2-2. Jumper Installation

BOOTSTRAP ADDRESS JUMPERS E16	. C D . . A . B	*A to B (standard) 773 000 A to C (alternate) 771 000
INTERRUPT LEVEL	Jumper Installed	Level
	JP1, JP2, JP3	BR4
	JP2, JP3	BR5 (Factory Set)
	JP1, JP3	BR6
	JP1	BR7
DEVICE ADDRESS JUMPERS D19		P to R (standard) 774 400 Interrupt Vector = 160 K to R (alternate) 775 400

*On an LSI-11/23 PLUS computer, bootstrap address 771 000 must be used.

PRE-INSTALLATION CHECKS

There are various LSI-11 configurations, many of which were installed before DEC made a hard disc available for LSI-11 based systems. Certain configurations require minor modifications before operating the disc system. These modifications are as follows:

A. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the controller if the DMA refresh logic on the REV11-C is enabled.

B. If the 4K memory on the DK11-F is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

C. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

D. If the REV11-C module is installed, cut the etch to pin 12 on circuit D30 (top of board) and add a jumper between pin 12 and pin 13 of D30.

E. If the system requires more than one backplane, place the REV-11 terminator in the last available location in the last backplane.

INSTALLATION

To install the controller module, proceed as follows:

CAUTION

Remove DC power from mounting assembly before inserting or removing the controller module.

Damage to the backplane assembly may occur if the controller module is plugged in backwards.

1. Select the backplane location into which the controller is to be inserted. Be sure that the disc controller is the lowest priority DMA device in the computer except if the DMA refresh/bootstrap ROM option module is installed in the system. The lowest priority device is the device farthest from the processor module. Note that the controller contains a bootstrap ROM.

   There are several backplane assemblies available from DEC and other manufacturers. Figure 2-2 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or in the first location in the first backplane of multiple backplane systems.

   It is important that all option slots between the processor and the disc controller be filled to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signals are complete to the controller slots. If there must be empty slots between the controller and any option board, the following backplane jumpers must be installed.

FROM	TO	SIGNAL
C0 × NS	C0 × M2	BIAK1/L0
C0 × S2	C0 × R2	BDMG1/L0
↑	↑	
Last Full Option Slot	Controller Slot	

2. Insert the controller into the selected backplane position. Be sure the controller is installed with the components facing row one, the processor.

   The controller module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

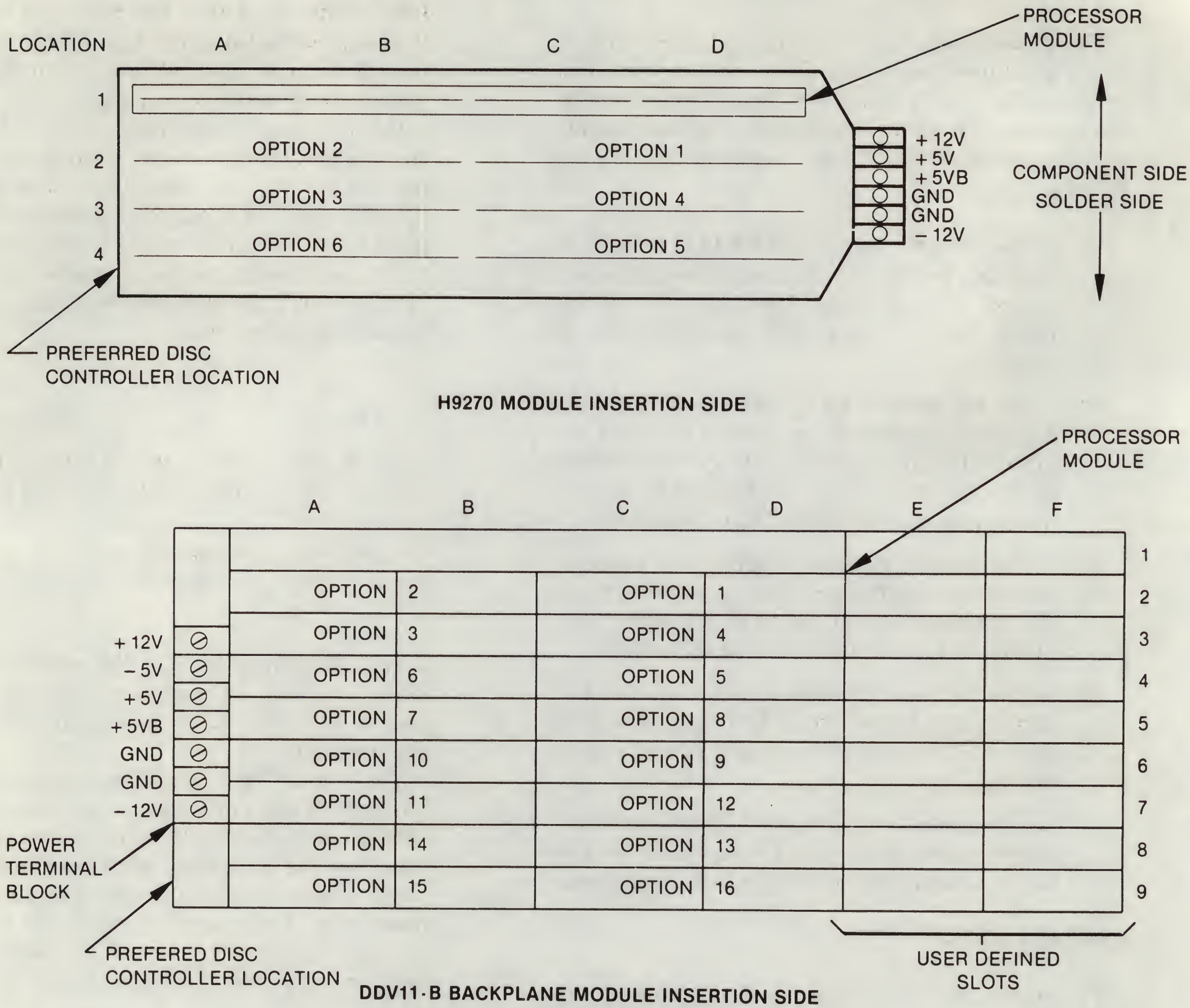
3. Feed the module connector end of the disc I/O cables into the controller module connectors. Ensure that pin 1 is matched with the triangle on the connector as shown in Figure 2-1. Install the cable connectors into the module connectors. Verify that the connectors are firmly seated.

4. Connect the disc-end of the I/O cables to the disc I/O connectors. Be sure that the bus terminator is installed at the last disc in the system.

5. Refer to the disc manual for operating instructions and apply power to the disc and computer.

6. Observe that the green diagnostic LED on the controller board is lit.

7. The system is now ready to operate. Refer to Section 3 for operating instructions, diagnostics, and formatting.



NOTE

MEMORY CAN BE INSTALLED IN ANY SLOT; IT IS NOT PRIORITY DEPENDENT AND DOES NOT NEED TO BE ADJACENT TO THE PROCESSOR.
CONTROLLERS ARE ALSO COMPATIBLE WITH H9273A MODULES.

Figure 2-2. Typical Backplane Configuration

GROUNDING

To prevent grounding problems, DILOG recommends standard ground braid be installed from the computer DC ground point to the disc drive DC ground point and also between disc drives at the DC ground points.

SECTION 3
OPERATION

INTRODUCTION

This section contains procedures for operating the computer system with the controller and a disc drive or drives. An understanding of DEC operating procedures is assumed. The material here is provided for "first time users" of disc subsystems and describes procedures for bootstrapping, formatting, and diagnostic testing.

PRECAUTIONS AND PREOPERATIONAL CHECKS

The following precautions should be observed before or during operation of the system. Failure to observe these precautions could damage the controller, the disc, the computer, could erase a portion or all of the stored software.

1. Verify that switches and jumpers are properly installed as described in Section 2.
2. Verify that the controller is properly positioned and is firmly seated in the backplane connector.
3. Verify that the cables between the controller and the drive, or drives, are properly installed.
4. When power is applied to the computer, ensure the green diagnostic LED lights.
5. Do not remove the controller when power is applied.
6. If the system does not operate properly, check the computer operating procedures and verify that the items in Section 2 of this manual have been performed.
7. Before formatting the drive, ensure that power is applied to the drive and the READY light is on (if applicable).

BOOTSTRAP PROCEDURE

The following assumes the system is in ODT mode. Note that the bootstrap can be used under processor Power Up Mode 2 conditions. Refer to the appropriate DEC manual for a discussion of the Power Up Modes. Further note that the disc drive does not need to be READY to enter the bootstrap.

Reset the system by pressing RESET or enter the following (characters underlined are output by the system; characters not underlined are input by the operator):

<u>@</u> 777300G or 771000G
Depends on jumper configuration in Section 2.

<u>*</u> Enter one of the following: DM0, DP0, DL0, DR0, MS0, MT0 or DY0 <CR>.

Definitions are as follows:

DM = RK06/07 Disc
DP = RP02/03 Disc
DL = RL01/02 Disc
DR = RM02/03 Disc
MS = TS11 Tape
MT = Tape
DY = RX02 Floppy Disc

Booting can be executed from logical units other than "0" by entering the desired logical unit number, i.e., DL1, DL2 . . .

FORMAT AND DIAGNOSTIC TEST PROGRAM

Description

DILOG's Universal Firmware and Diagnostic Program permits the user to format a disc pack for his particular application; compensate for media errors; and test the controller and drive. When formatted, the disc may be partitioned horizontally or vertically. Either way, the pack is divided into logical units which the computer recognizes. The user may select one of three types of partitioning: 1-head, 2-head or vertical.

The constraints for selection are:

Subsystem:

- Maximum number of logical units is 4.

1-head:

- Maximum number of heads (surfaces) is 4.
- Maximum size of logical units is 20,480 records.

2-head:

- Maximum number of heads (surfaces) is 8.
- Number of fixed and removable heads (surfaces) must be even.
- Maximum size of logical units is 20,480 records.

Vertical:

- Maximum size of logical units is 20,480 records.

The disc pack is divided vertically by cylinders and horizontally by heads (or data surfaces). Each head (surface) is further divided into tracks. A track is addressed by cylinder number and head number. Tracks are further divided into sectors (or records or blocks) which the computer recognizes as increments within a logical unit. Sectors consist of overhead bytes (such as address, sync, error correction) and data bytes. The standard number of data bytes, bytes usable by the computer, is 512 data bytes per sector. Figure 3-1 illustrates vertical and head partitioning.

Table 3-1 is a partial list of disc drives and specifications for partitioning. Column 1 lists the manufacturers. Column 2 lists the model numbers. Column 3 lists the sectors (also called records and blocks) per track. Column 4 lists the number of heads (surfaces) per drive. Column 5 lists the cylinders per drive. Columns 6 and 7 list the emulations and the number of megabytes and sectors per logical unit. Column 8 lists the megabyte capacity and number of sectors of the last logical unit partitioned. Column 9 lists the number of alternate tracks per physical drive.

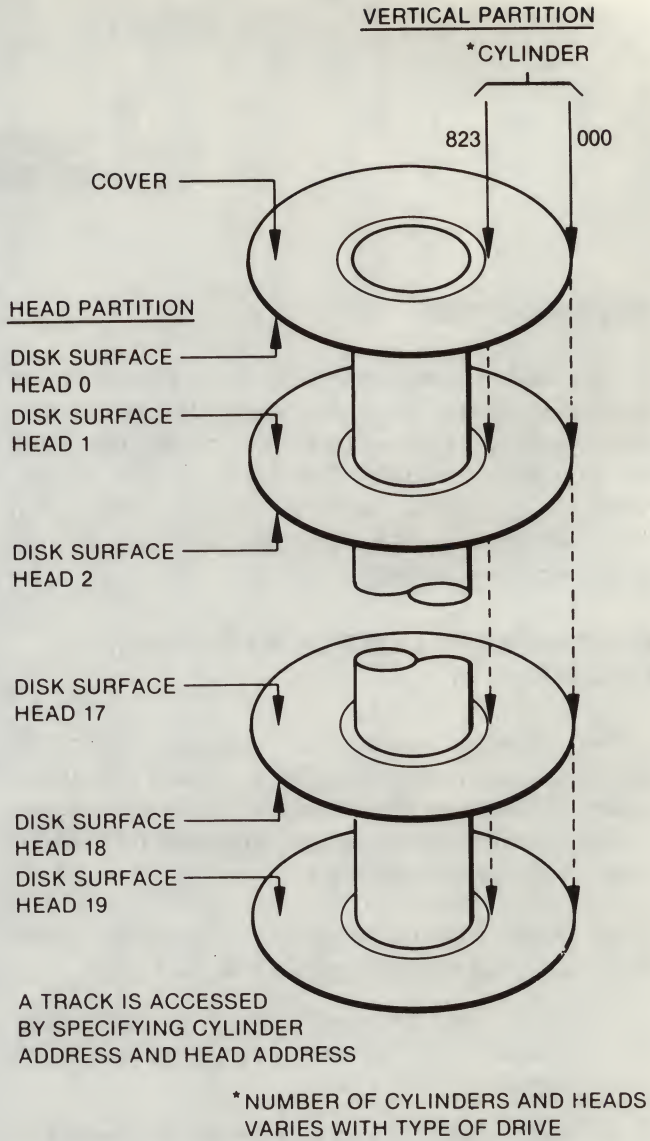


Figure 3-1. Partitions

Parameters for disc drives not listed in Table 3-1 may be determined from manufacturer's specifications and the following: Determine the number of bytes per track from the manufacturer's specification. The number of bytes per sector (data and overhead) for DILOG controllers is 568. Divide the number of bytes per track by the number of bytes per sector. Drop the remainder. This value is the number of sectors per track. Then, number of sectors per track × number of heads × number of cylinders per drive = number of sectors per drive.

The program will prompt for the following to partition a drive:

- Does the drive have removable media
- Number of sectors/track
- Number of heads/drive
- Number of cylinders/drive

Table 3-1. Values for Partitioning With Universal Firmware (RL01/RL02)

(1) Manufacturer	(2) Model Number	(3) Sectors (Records) (Blocks) Track	(4) Heads (Data Surfaces) Drive Removable	Fixed	(5) Cylinders/ Drive	(6) Total Logical Units RL02 Units 10.48MB 20,480 Sectors	(7) RL01 Units 5.24MB 10,240 Sectors	(8)** Last Logical Unit MB	Sectors	(9) Physical Drive Alternate Tracks
BASF	6172	23	0	3	600		4	5.26[a]	10281	12
						2	1	00.07[b]	138	12
CDC	9455 Lark I	32	2	2	202		3	2.49[b]	4864	16
						1	1	2.49[b]	4864	16
KENNEDY	6172	23	0	3	614	1	2	01.47[b]	2880	12
MITSUBISHI	M2860-1	23	0	3	548		4	03.42[b]	6693	12
						1	1	08.72[a]	17043	12
PRIAM	3450	23	0	5	525	2	1	09.59[a]	18745	20
PRIAM	3350-33	35	0	3	555	2	1	08.54[a]	16695	12

*For a 1-head partition, the value of cylinders/drive = tracks/surface

**Calculated using 4 alternates.

[a] Greater than standard RL01.

[b] Less than standard RL01.

The user may require alternate cylinders, or spares, to compensate for media flaws, soft errors, or marginal drive conditions. All three types of partitioning in the program make provisions for sparing. The program accounts for alternates when calculating the number and size of logical units.

If the number of logical units is to be changed, the configuration switches should also be changed before completion of format and test.

The descriptions below indicate what parameters will be changed as various elements are changed; for example, if the number of logical units is changed, the size of the logical units will change.

1-Head Partition

Parameters for 1-head partitioning are determined as follows:

1. Determine the number of alternate tracks required for each logical unit. Subtract the number of alternates from the number of tracks per head. The number of tracks per head is the same number as cylinders per drive, Table 3-1, column 5. This value is the *usable* tracks per head. Then,
2. Sectors per track × (tracks per head minus alternates) = number of sectors per logical unit.
3. Sectors per logical unit × 512 = Megabyte capacity per logical unit.
4. Number of heads = Number of logical units.

For example, the BASF 6172 has 23 sectors, 3 heads, and 600 tracks/head (cylinders/drive). To simplify, assume there are four alternates required.

1. 600 tracks/head − 4 alternates = 596 usable tracks/head.
2. 23 × 596 = 13708 sectors/logical unit.
3. 13708 × 512 = 7.01 MBytes/logical unit.
4. 3 Heads = 3 logical units.

When the program partitions the above, the following will appear:

LOGICAL UNIT	PHYSICAL DRIVE	MEGABYTES	RECORD SIZE
DL0	0	07.01	13708
DL1	0	07.01	13708
DL2	0	07.01	13708

PHYSICAL DRIVE 0 HAS 12 ALTERNATE TRACKS

2-Head Partition

The parameters for 2-head partitioning are the same as for 1-head except that the number of sectors/logical unit is multiplied by two:

1. Determine the number of alternate tracks required for each logical unit. Subtract the number of alternates from the number of

tracks per head. The number of tracks per head is in Table 3-1, Column 5. Then,

2. Sectors per track × (tracks per head minus alternates) × 2 = Number of sectors per logical unit.
3. Sectors per logical unit × 512 = Megabyte capacity per logical unit.
4. Number of heads per drive divided by 2 = Number of logical units per drive.

For example, the CDC Model 9455 has 32 sectors, 4 heads, and 202 tracks/head (cylinders/drive). To simplify, assume there are four alternates required.

1. 202 tracks/head — 4 alternates = 198 usable tracks/head.
2. 32 × 198 × 2 = 12672 sectors/logical unit.
3. 12672 × 512 = 6.48 MBytes/logical unit.
4. 4 Heads per drive divided by 2 = 2 logical units.

When the program partitions the above, the following will appear:

LOGICAL UNIT	PHYSICAL DRIVE	MEGABYTES	RECORD SIZE
DL0	0	6.48	12672
DL1	0	6.48	12672

PHYSICAL DRIVE 0 HAS 16 ALTERNATE TRACKS

Vertical Partition

With vertical partitioning, the user may select standard (Table 3-1) or nonstandard size units. If nonstandard units are selected, the user may select either the number of logical units or the size of the logical units. If the number of logical units is selected, the logical units will be of equal size. If the size of logical units is selected, all logical units may not be of equal size.

Parameters for vertical partitioning are determined as follows:

User specifies the *number* of logical units (all logical units are of equal size):

1. Determine the required number of alternate cylinders per drive. Subtract the number of alternates from the number of cylinders per drive (Column 5). This value is the *usable* cylinders per drive.
2. Determine the number of logical units per drive required. Then,
3. Number of usable cylinders per drive divided by number of logical units required = Number of cylinders per logical unit. The remainder is assigned as an alternate.
4. Number of cylinders per logical unit × sectors per track × number of heads = Number of sectors per logical unit.
5. Number of sectors per logical unit × 512 = Megabyte capacity per logical unit.

User specifies the *size* of logical units in sectors per logical unit (the last logical unit will be a different size):

1. Determine the required number of alternate cylinders per drive. Subtract the number of alternates from the number of cylinders per drive (Column 5). This value is the usable cylinders per drive.
2. Determine the required number of sectors (blocks) per logical unit. Then,
3. Sectors per track (Column 3) × number of heads (Column 4) divided into sectors per logical unit = cylinders per logical unit. If there is a remainder, the number of cylinders per logical unit is rounded off to the next higher number.
4. Number of usable cylinders divided by cylinders per logical unit = number of logical units. If there is a remainder, the number of logical units is rounded off to the next higher number.
5. Number of cylinders per logical unit × number of full (equal size) logical units = Number of cylinders full (equal size) logical units.
6. Number of usable cylinders per drive minus number of cylinders in full logical units = Number of cylinders in partial logical unit.

For standard units, if RL02 units, vertical partition, and 4 alternates are selected for the Priam 3350-33, the program will divide the sectors into standard size units and, in effect, ask the user if the remainder (159 cylinders, 08.54 MByte in this case) should be a smaller size unit or assigned as alternates. If 0 alternates are requested, the following will be displayed:

LOGICAL UNIT	PHYSICAL DRIVE	MEGABYTES	RECORD SIZE
DL0	0	10.48	20480
DL1	0	10.48	20480
DL2	0	8.54	16695

PHYSICAL DRIVE 0 HAS 12 ALTERNATE TRACKS

Two-Drive Selection

When two drives are selected for any partition, it is important to keep in mind the constraints stated previously; for example, a subsystem may not exceed 4 logical units.

The CDC 9455 (Lark) and the Mitsubishi M2860-1 are a mix-and-match combination; both may be partitioned as a subsystem. With vertical partitioning, standard RL02 units, no alternates requested, the drives may be partitioned as follows:

LOGICAL UNIT	PHYSICAL DRIVE	MEGABYTES	RECORD SIZE
DL0	0	10.48	20480
DL1	0	2.49	4864
DL2	1	10.48	20480
DL3	1	8.72	17043

PHYSICAL DRIVE 0 HAS 16 ALTERNATE TRACKS
PHYSICAL DRIVE 1 HAS 12 ALTERNATE TRACKS

Partitioning Program

The name of the program is RLXXXD, where XXX is the revision number of the program.

Figure 3-2 is a flow diagram of the program. The statements in quotes are program prompts. The pentagonoid symbols with a letter and number, such as "A1," are reference points for breaks in the flow. The "A" designations refer to the first page (Format) and the "B" designations refer to the second page (Change Parameters). The following descriptions refer to the first (Format) page of the diagrams.

When the program is initialized the following display will appear on the terminal:

DILOG'S UNIVERSAL FIRMWARE AND DIAGNOSTIC PROGRAM VERIFIES PROPER FUNCTIONING OF THE DILOG RL01/RL02 EMULATING DISC CONTROLLER AND FORMATS THE DISC TO YOUR SPECIFICATIONS.

YOUR DEFAULT PARAMETERS ARE:

SECTORS ____
HEADS ____
CYLINDERS ____
ALTERNATES ____
SIZE OF LOGICAL UNITS (RECORDS) ____

The parameters displayed are calculated for the efficiency of most applications. The units of measure are as follows: sectors/track; heads/drive; cylinders/drive; alternates/drive; and the size of logical unit in sectors/logical unit.

The next display will be:

```
***************************************
*****  RESTART ADDRESS IS 2000  *****
******  ^X RESTARTS PROGRAM  ******
****  ^C RESTARTS CURRENT TEST ****
***************************************
```

To restart, press the CTRL and X keys at the same time, or CTRL and C.

The next query is:

ARE YOU RUNNING THE DIAGNOSTIC VIA A CRT (Y OR N)?

If the answer is No, the CRT will not display the current cylinder address during the test program.

The next prompt is:

ENTER NUMBER OF DRIVES

Enter 1 or 2. If 1 is entered, the next queries will refer only to Drive 0. If 2 drives are selected, the program will prompt for Drive 0 and Drive 1.

The next displays will be:

ENTER DEVICE ADDRESS <774400>?
ENTER INTERRUPT VECTOR <000160>?

The address is factory set unless the user requested an alternate address (see Section 2).

The menu of drives will appear next, with the following:

********DRIVE 0********

ENTER NUMBER CORRESPONDING TO DISC DRIVE
OR
SELECT ANOTHER PAGE
N=NEXT PAGE P=PREVIOUS PAGE E=ENTER PARAMETERS

From the menu, the appropriate drive may be selected. If E is pressed, the program will prompt for drives not listed in the menu or will prompt to change parameters in case of conflicts in constraints.

Note

The program responds with the minimum number of inquiries; for example, if a drive is selected from the menu, the program will not prompt for the number of sectors, heads and cylinders, because these responses are predetermined.

If a drive is selected from the menu, the next display will be:

DO YOU WISH TO CHANGE FORMAT PARAMETERS (DRIVE 0)?

Note

The format parameters are those last entered. Each time there is a change, the program will retain that change.

If the response is No, the next display will show the configuration. An example is as follows:

DISC SYSTEM CONFIGURATION

LOGICAL UNIT	PHYSICAL DRIVE	MEGABYTE	RECORD SIZE
DL0	0	5.24	10248
DL1	0	5.24	10248
DL2	0	5.24	10248
DL3	0	5.07	9912

PHYSICAL DRIVE 0 HAS 0 ALTERNATE TRACKS
PHYSICAL DRIVE 1 HAS 16 ALTERNATE TRACKS

ARE YOU SURE?

If the answer is Yes, the program will skip to the Test section. If the answer is No, the program will repeat.

The following descriptions refer to the second (Change Parameters) page of the diagram.

If the answer is Yes to the prompt:

DO YOU WISH TO CHANGE FORMAT PARAMETERS (DRIVE 0)?

the next prompt will be:

CHANGE NUMBER OF SECTORS (Y OR N)?
CHANGE NUMBER OF HEADS (Y OR N)?
CHANGE NUMBER OF CYLINDERS (Y OR N)?

These prompts are for adding a drive that is not on the menu. The values (after HOW MANY?) to be entered are in the drive manufacturer's manual. The next prompt of change parameters is for drives which are or are not on the menu:

CHANGE NUMBER OF ALTERNATES (Y OR N) <4>?

The standard number of alternates selected is 4. If Yes, HOW MANY? will appear. The next query is:

CHANGE TYPE OF PARTITION (Y OR N) <VERTICAL>?

If the answer is Yes, the program will prompt with 1-HEAD, 2-HEAD, OR VERTICAL? If 1-head or 2-head is selected there will be no further queries. Next to appear is:

STANDARD SIZE UNITS (Y OR N)?

If Yes, the program will prompt with selection of RL01 or RL02. If RL02 is selected, the program will divide the record size into RL02 units, and the remaining records will be an RL01 unit. Standard sizes are shown in Table 3-1.

After the program divides the records into RL01 or RL02 units, there may be remaining cylinders. The program gives the user the option of assigning the remainder as alternates or creating another logical unit. The prompt is as follows:

AFTER CALCULATING STANDARD SIZE UNITS, YOU HAVE ____ CYLINDERS NOT ALLOCATED (____ MBYTE). IF YOU WOULD LIKE, I COULD CREATE ANOTHER UNIT, WHICH WOULD BE SMALLER THAN YOUR STANDARD SIZE UNIT OR I COULD ALLOCATE THE CYLINDERS AS ALTERNATES.

PLEASE ENTER THE NUMBER OF CYLINDERS YOU WOULD LIKE ME TO ALLOCATE AS ALTERNATES. ANY REMAINDER WILL BE ALLOCATED AS ANOTHER UNIT.

ENTER >

If the number of alternates previously selected is adequate (standard number of alternates is 4), enter 0.

If standard size units are not selected, the next display will be:

CHANGE SIZE OF LOGICAL UNIT (RECORDS) (Y OR N) <XXXXX>?
CHANGE NUMBER OF LOGICAL UNITS (Y OR N) <X>?

If Yes is answered to the first question, the program will not ask the second. The above sequence will repeat for the second drive:

DO YOU WISH TO CHANGE FORMAT PARAMETERS (DRIVE 1)?

If the constraints are not violated, the Disc Subsystem Configuration and ARE YOU SURE? will appear. If the response is Yes, the program will begin the test sequence. If the subsystem constraints are violated, a message similar to the following will appear:

FORMAT PARAMETER CONFLICTS SUBSYSTEM

DRIVE 0 IS CONFIGURED FOR 4 LOGICAL UNITS
DRIVE 1 IS CONFIGURED FOR 4 LOGICAL UNITS
MAXIMUM NUMBER OF LOGICAL UNITS ALLOWED IS 4

Check the constraints at the beginning of this section, and check Table 3-1 for record sizes. If this conflict can be resolved, the number of logical units may be changed for each drive. To provide logical units of equal size on both drives, the number of logical units may be changed to 2 on each drive.

Examples of errors on a single drive when changing the type of partition are as follows:

FORMAT PARAMETER CONFLICTS
DRIVE 0

MAXIMUM NUMBER OF HEADS WITH
1-HEAD PARTITION IS 4

or

FORMAT PARAMETER CONFLICTS
DRIVE 1

MAXIMUM NUMBER OF HEADS WITH
2-HEAD PARTITION IS 8

or

FORMAT PARAMETER CONFLICTS
DRIVE 0

MAXIMUM NUMBER OF HEADS MUST BE
AN EVEN NUMBER WITH 2-HEAD
PARTITION

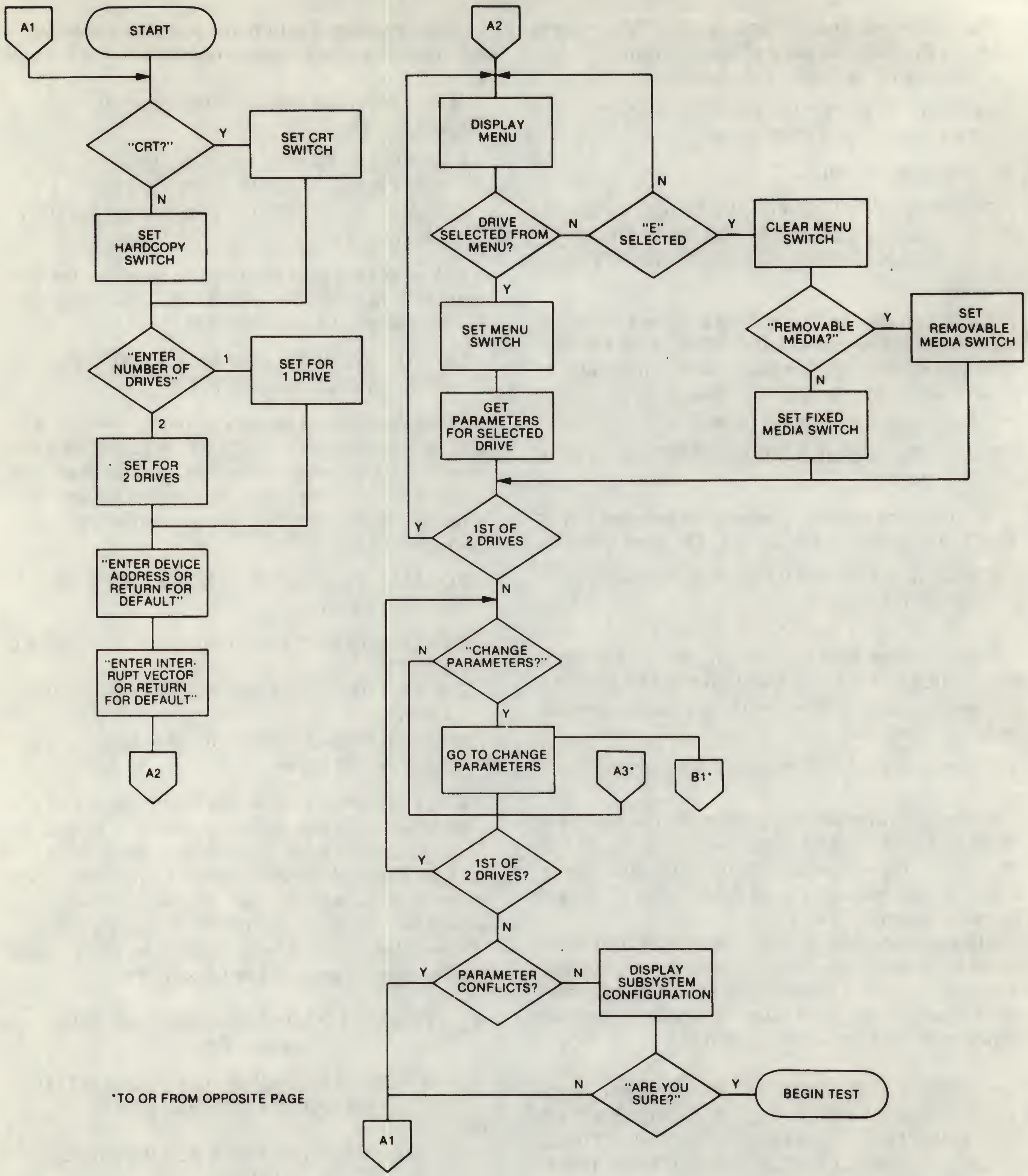


Figure 3-2(A). Universal Formatting

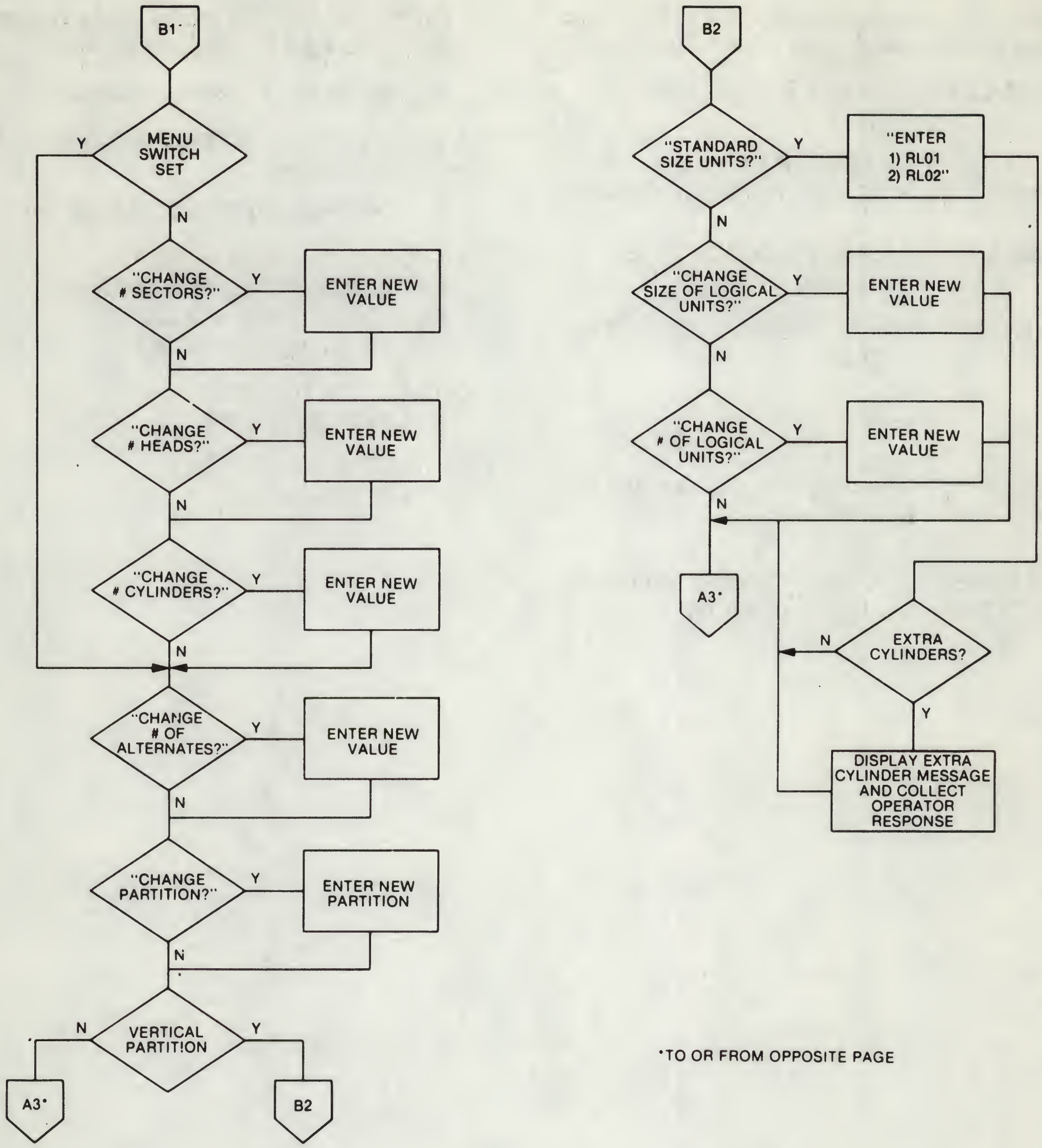


Figure 3-2(B). Universal Formatting—Change Parameters

Examples of errors on a single drive when changing the size of the logical units is as follows:

FORMAT PARAMETER CONFLICTS
DRIVE 0

LOGICAL UNIT SIZE IS 40,320
MAXIMIM LOGICAL UNIT SIZE IS 20,480

or

FORMAT PARAMETER CONFLICTS
DRIVE 0

LOGICAL UNIT SIZE IS BIGGER THAN THE DISC

Mapping

The algorithm for mapping, that is, what the controller should map, is as follows:

$$\frac{\text{Record Number}}{\text{Sector/Cylinder}} = \text{Correct Cylinder Address} + \text{Remainder (1)}$$

$$\frac{\text{Remainder (1)}}{\text{Sector/Track}} = \text{Correct Head Address} + \text{Remainder (2)}$$

$$\text{Remainder (2)} = \text{Sector Address}$$

A mapping error is displayed during the Random Read test as follows:

*****MAPPING ERROR*****

RECORD NUMBER = XXX
SECTOR/CYLINDER = XXX
SECTOR/TRACK = XXX
DRIVE NUMBER = XXX

CORRECT ADDRESS
CYLINDER = XXX

CONTROLLER ADDRESS
CYLINDER = XXX

Diagnostic Test Program

The format/test program contains the following:

1. TEST CONTROLLER
   A. Registers
   B. Data Buffer
2. TEST DISC DRIVE
   A. Disc Ready
   B. Disc Restore (seek to cylinder 0)
3. FORMAT
   A. Write Headers
   B. Read Headers
   C. Write Data Test Pattern
   D. Read Data Test Pattern
4. SEQUENTIAL READ
5. SELECTED READ
6. RANDOM SEEK, READ
7. RANDOM SEEK, WRITE, READ, AND COMPARE
8. ASSIGN ALTERNATE TRACK

Test Controller

The program will automatically test the controller registers and data buffer. The program will only display error messages during this test; the display will be:

DATA BUFFER ERROR

or the mnemonics of the controller registers and the location and contents (in octal). The display of the registers is followed by an error identification message to aid in isolating the specific problem.

Note

Whenever an error occurs and the registers are displayed, an audio alarm signal is generated to notify the operator.

The error identification message is as follows:

DISC ADDRESS
SECTOR ___ HEAD ___ CYLINDER ___
DRIVE ___
TYPE OF COMMAND ___
CONTROL STATUS ERROR ___
DRIVE STATUS ___

Listed are the sector, head, cylinder and drive (in decimal) where the error occurred. An example of Type of Command is Read Data Command. An example of Control Status is Seek Error.

The program will next display:

USE C TO CONTINUE
USE O TO TRANSFER TO ODT
USE L TO REBOOT YOUR SYSTEM

"C" is used to continue the test. "O" is used for ODT (on-line debugging technique). "L" is used to initiate the system bootstrap.

Test Disc Drive

After the controller test is performed, the program will automatically test the drive for ready and restore. The disc address is not displayed during this test. If the disc will not restore, the program will display the register for cylinder 0.

Format

The operator may format the entire subsystem, each drive, or selected logical units. Program messages are as follows:

FORMAT ENTIRE SUBSYSTEM (Y OR N)?
FORMAT DRIVE 0 (Y OR N)?
FORMAT DRIVE 1 (Y OR N)?
FORMAT DL0 (Y OR N)?
FORMAT DL1 (Y OR N)?
FORMAT DL2 (Y OR N)?
FORMAT DL3 (Y OR N)?
FORMAT ALTERNATE CYLINDERS DRIVE 0 (Y OR N)?
FORMAT ALTERNATE CYLINDERS DRIVE 1 (Y OR N)?

Note

Before any write operation, the program will display ARE YOU SURE? This aids the operator in preventing reformatting of a previously formatted logical unit (possibly destroying good data).

During formatting the following messages will appear sequentially:

WRITING HEADERS
CURRENT CYLINDER ADDRESS ___

READING HEADERS
CURRENT CYLINDER ADDRESS ___

WRITING DATA TEST PATTERN ___
CURRENT CYLINDER ADDRESS ___

READING DATA TEST PATTERN ___
CURRENT CYLINDER ADDRESS ___

When reading and writing headers, the program will display the cylinder addresses sequentially. The test pattern tests are also sequentially selected, and the cylinder address displayed will correspond to the current address being read.

After each logical unit is formatted, the display will be:

DM___ FORMAT AND VERIFICATION COMPLETE

Sequential Read

For this test, the display will be:

SEQUENTIAL READ (ALL CYLINDERS AND HEADS)?

If the response is No, the program will jump to the Selected Read test. If the response is Yes, the current cylinder address is displayed as each cylinder is read. If an error is detected, the register contents and location are displayed with the error identification message, and the following:

ASSIGN ALTERNATE CYLINDER?

If no alternates (spares) are available, the following will be displayed:

NO ALTERNATE CYLINDER AVAILABLE

When marking or assigning alternate tracks, the following error messages may occur:

TRACK HAS ALREADY BEEN MARKED DEFECTIVE
TRACK HAS ALREADY BEEN MARKED ALTERNATE

Selected Read

For this test, the display will be:

READ DL0? (Y OR N)?

If the response is No, the next logical unit will be displayed. If the response is Yes, the current cylinder address is displayed and each cylinder is read. If an error is detected, the register contents and location are displayed with the error identification message. The ASSIGN ALTERNATE TRACK message appears, and error messages if the track has been marked DEFECTIVE or ALTERNATE.

Random Seek, Read

For this test, the display will be:

RANDOM SEEK, READ OF DRIVE (ALL CYLINDERS AND HEADS)?

This test selects a random cylinder, logical unit, and a sector address within the cylinder. The test then reads data and tests for errors. All logical units are used in this test. Alternate cylinders cannot be assigned during this test. The terminal keyboard Space (SP) character is used to exit this test.

If an error is detected, the register contents and locations are displayed with the error identification message.

This check also ensures controller mapping is correct. The desired address and the actual address will be displayed with the drive's physical characteristics.

Random Seek, Write Data, Read Data, Compare Test

If the response to ALL CYLINDERS AND HEADS? is No, each logical unit will appear in sequence until the response is Yes.

DL0?
DL1?
DL2?
DL3?

This test selects a random cylinder address and random sector address and writes five sectors (2560 bytes) of random data. The data written is then read into CPU memory and compared for read errors. This test allows logical units to be tested. The terminal keyboard Space (SP) character is used to exit from this test.

This test ensures that the controller is executing the Write Check command correctly and that the controller is zero-filling the disc correctly.

Assign Alternate Track

This test may be used if the disc drive manufacturer provides a map describing defective tracks.

The message is:

ASSIGN ALTERNATE TRACK FOR DEFECTIVE TRACK (Y OR N)?

If the response is No, the program will revert to:

USE R TO REPEAT
USE O TO ODT
USE L TO REBOOT

If the response is Yes, the display will be:

PHYSICAL DRIVE (0 or 1)?
(only if two drives are present)

CYLINDER ADDRESS (0 TO ____)

Enter the cylinder address, in decimal, of the defective track. If the cylinder address entered is incorrect, the message will be repeated.

The next message will be:

HEAD ADDRESS (0 TO ____)

Enter the head address, in decimal, of the defective track. If the head address entered is incorrect, the message will be repeated.

The next message will be:

MAP OUT
CYLINDER ____ HEAD ____
ARE YOU SURE (Y OR N)?

If No, the program will repeat the first message of this test. If Yes, an alternate cylinder is assigned and the message is:

ALTERNATE CYLINDER ASSIGNED

Other messages to appear may be:

TRACK ALREADY MARKED DEFECTIVE

or

TRACK ALREADY MARKED ALTERNATE

The program will then repeat the first message of this test.

SECTION 4
PROGRAMMING

PROGRAMMING DEFINITIONS

Function—The expected activity of the disc system (write, seek, read, etc.).

Command—To initiate a function (halt, clear, go, etc.).

Instruction—One or more orders executed in a prescribed sequence that cause a function to be performed.

Address—The binary code placed in the BDAL0-15 lines by the bus master to select a register in a slave device. Note memory other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

Register—An associated group of memory elements that react to a single address and store information for use by other assemblies of the total computer system.

DISC CONTROLLER FUNCTIONS

The disc controller performs 8 basic functions. In addition, when bit 15 of the Multipurpose register is off, the function Write Data becomes Write Header. A function is initiated by a GO command after the processor has issued a series of instructions that store funtion-control information into controller registers. To accept a command and perform a function, the controller must be properly addressed and the disc drive(s) must be powered up, be at operational speed, and be ready.

The 8 functions performed by the controller are established by bits 01, 02 and 03 of the Control/Status register (RLCS). The functions and bit codings are given in Table 4-1. Descriptions of the functions are given in the following paragraphs.

Clear Controller

This function clears controller logic to the initial conditions and terminates data transfers at the end of the sector currently being transferred. This function is entered when the controller is initially cleared or when the function register contents equal 0. If GO is set while the contents of the function register equal zero, Clear Controller is generated. The Clear command can be executed even if the controller is in the NOT READY state.

Table 4-1. Controller Functions

Bit			Octal Code	Description
03	02	01		
0	0	0	(0)	Clear Controller
0	0	1	(2)	No Op
0	1	0	(4)	Get Status
0	1	1	(6)	Seek
1	0	0	(10)	No Op
1	0	1	(12)	Write Data*
1	1	0	(14)	Read Data*
1	1	1	(16)	Read Data (without header check)

Write format if bit 15 is off in the Multipurpose Register — word count (774 406)

**Read format if bit 15 is off in the Multipurpose Register — word count (774 406)

Get Status

This function is used to get drive status into the Multipurpose register (RLMP). Bit 5 of the Disc Address register (RLDA) is used to read/write the data buffer. Bit 4 performs a Restore operation.

Seek

The controller responds to the Seek function if the octal code 06 is loaded in the RLCS register and Go is set; all the proper responses are made to the RL01/02 handler by the controller to indicate the proper completion of this function, Seek Complete interrupt, etc. However, the controller does not actually issue a Seek command to the disc drive. This function was originally implemented when each physical disc drive was one logical unit. Now that multiple logical units are in one physical drive, the function is no longer practical. Furthermore, all read and write functions include automatic seeks.

Write Data

The Write Data function includes a seek to the desired starting disc address (cylinder and track). The function is executed by loading octal code 12 into RLCS and setting Go, causing the controller to write one or more data records on the addressed

disc. Writing starts at the drive, cylinder, head and sector addresses specified by the RLDA register. The amount of data written is specified by the (RLMP) Word Count register. Write data transfers start from the memory address specified by the RLBA register. Each data word transferred increments the Bus Address and Word Count registers. When the (RLMP) Word Count overflows, data transfer is completed and controller action is terminated at the end of the current disc sector. As data is written, a CRCC is calculated and written as the last word of each sector. Prior to writing, the header record is read to verify proper head positioning.

If bit 15 is off in RLMP (Word Count), the function performed is Write Header.

Read Data

The Read Data function causes the controller to read one or more data records from the disc drive. The read function includes a seek to the starting disc address (cylinder, head, sector) and is initiated by loading octal code 14 into the RLCS register and setting Go. Data transfers from the disc are stored in memory starting with the memory address specified by the RLBA register. The amount of data read is specified by the RLMP Word Count register. Each data word transferred increments the Bus Address and Word Count registers. The contents of the RLMP Word Count register at the beginning of the transfer specify the number of words to be transferred. When the RLMP Word Count overflows, data transfers stop.

While data is being read, the controller calculates a CRC. At the end of the sector, the calculated CRC is compared with the CRC read from the sector. If they disagree, bit 11 of RLCS is set.

Prior to reading the data record the header record is read to verify proper head position.

If bit 15 is off in RLMP (Word Count), the function performed is Read Header.

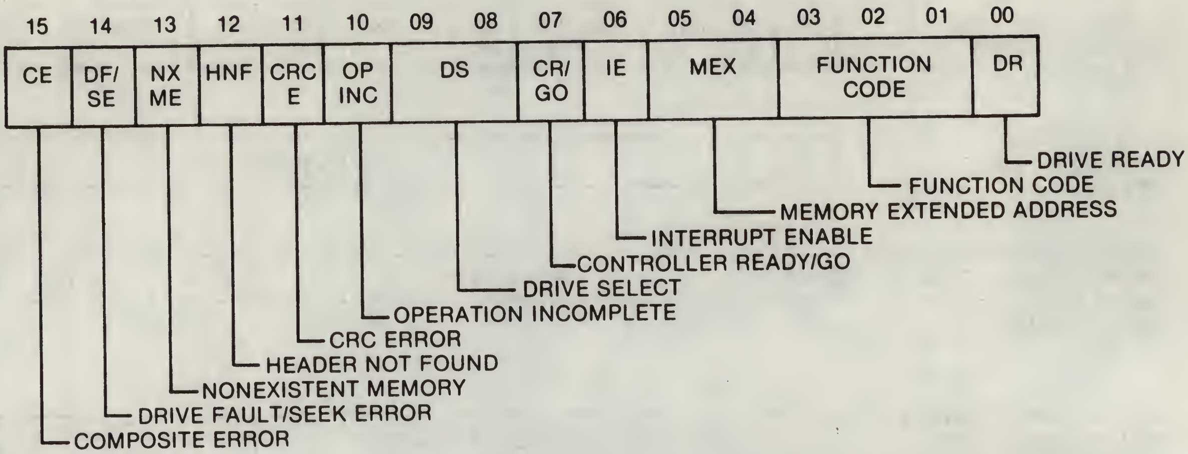
CONTROL REGISTERS

All software interaction between the disc controller, the processor, and the processor memory is accomplished by four registers which are read as 12 registers in the disc controller. These registers are assigned memory addresses and can be read or written into (except as noted) by instructions that refer to the respective register addresses. The 12 controller registers, their addresses, their mnemonics, and their bit assignments are shown in Figure 4-1.

<table>
<tr><td></td><td colspan="8">MSB</td><td colspan="8">LSB</td></tr>
<tr><td>BIT POSITION</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>09</td><td>08</td><td>07</td><td>06</td><td>05</td><td>04</td><td>03</td><td>02</td><td>01</td><td>00</td></tr>
<tr><td>CONTROL/STATUS REGISTER (RLCS) 774 400</td><td>CE</td><td>DF/ SE</td><td>NX ME</td><td>HNF</td><td>CRC E</td><td>OP INC</td><td colspan="2">DS</td><td>CR/ GO</td><td>IE</td><td colspan="2">MEX</td><td colspan="3">FUNCTION CODE</td><td>DR</td></tr>
<tr><td>BUS ADDRESS REGISTER (RLBA) 774 402</td><td colspan="16">BUS ADDRESS</td></tr>
<tr><td>DISC ADDRESS REGISTER (RLDA) DURING READ/ WRITE COMMANDS (RL01/ RL02 EMULATION) 774 404</td><td colspan="9">CYLINDER ADDRESS</td><td>HS</td><td colspan="6">SECTOR ADDRESS</td></tr>
<tr><td>DISC ADDRESS REGISTER (RLDA) DURING SEEK COMMAND 774 404</td><td colspan="9">CYLINDER ADDRESS DIFFERENCE</td><td colspan="2">RSVD</td><td>HS</td><td>0</td><td>DIR</td><td>0</td><td>1</td></tr>
<tr><td>DISC ADDRESS REGISTER (RLDA) DURING GET STATUS 774 404</td><td colspan="10">NOT USED</td><td>RW DB</td><td>RD</td><td>RDE</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>DISC ADDRESS REGISTER (RLDA) DURING FORMAT COMMANDS (BIT 15 OFF IN RLMP REGISTER) 774 404</td><td colspan="4">HA</td><td>ESG</td><td>IAS</td><td colspan="10">CYLINDER ADDRESS</td></tr>
<tr><td>MULTIPURPOSE REGISTER (RLMP) DURING READ/WRITE COMMANDS FOR WORD COUNT 774 406</td><td>DF</td><td colspan="15">2'S COMPLEMENT WORD COUNT</td></tr>
<tr><td>MULTIPURPOSE REGISTER (RLMP) DURING READ HEADER COMMAND 774 406</td><td colspan="9">CYLINDER ADDRESS</td><td>HA</td><td colspan="6">SECTOR ADDRESS</td></tr>
<tr><td>MULTIPURPOSE REGISTER (RLMP) DURING GET STATUS COMMAND 774 406</td><td colspan="2">DF</td><td>DWP</td><td>DSE</td><td colspan="4">0</td><td>RL 02</td><td colspan="2">0</td><td>DR</td><td>1</td><td>DR</td><td>0</td><td>1</td></tr>
<tr><td>MULTIPURPOSE REGISTER (RLMP) DURING READ/WRITE DATA BUFFER 774 406</td><td colspan="16">DATA BUFFER</td></tr>
<tr><td>MULTIPURPOSE REGISTER (RLMP) DURING READ UNMAPPED CYLINDER COMMAND 774 406</td><td colspan="6">NOT USED</td><td colspan="10">CYLINDER ADDRESS</td></tr>
<tr><td>ADDRESS EXTENSION REGISTER (RLBAE) 774 410</td><td colspan="10">0</td><td colspan="6">ADDRESS EXTENSION 21-16</td></tr>
</table>

Figure 4-1. Register Summary

CONTROL/STATUS REGISTER (RLCS)
774 400



The address of RLCS is 774 400. This register indicates drive conditions, decodes drive commands, and provides overall control functions and error indications.

BIT(S) DEFINITIONS

00 DRIVE READY—When set, this bit indicates that the selected drive is ready to receive a command. This bit is cleared when a function is initiated and is reset when the function is completed.

01-03 FUNCTION CODE—These bits are set by software to indicate the command to be executed.

BIT 03 02 01	OCTAL CODE	DESCRIPTION
0 0 0	(0)	No Operation (Clear Controller)
0 0 1	(2)	Write Check
0 1 0	(4)	Get Status
0 1 1	(6)	Seek
1 0 0	(10)	Read Header
1 0 1	(12)	Write Data**
1 1 0	(14)	Read Data***
1 1 1	(16)	Read Data

** = Write Format if Bit 15 OFF in Multipurpose registers (774 406) (Word Count)
*** = Read Headers if Bit 15 OFF in Multipurpose Register (774 406)

04-05 MEMORY EXTENDED ADDRESS—These bits are the extended bus address bits for systems with memories larger than 32K 16-bit words, and are used in conjunction with the RLBAE register. These bits increment each time RLBAE overflows.

06 INTERRUPT ENABLE—This read/write bit causes the controller to raise an interrupt request when a disc operation is completed or if an error occurs. This bit is cleared by the Init or Reset functions.

07 CONTROLLER READY/GO—When cleared by software, this bit indicates that the command in bits 1-3 is to be executed. When set, this bit indicates that the controller is ready to accept another command.

08-09 DRIVE SELECT—These bits determine which drive will communicate with the controller via the drive bus.

10 OPERATION INCOMPLETE—This bit, when set, indicates that an operation was attempted when the contents of the register specifying the sector address were not within the proper range, or when the requested sector was not found. This bit is reset by the Init or Reset functions.

11 CRC ERROR—This bit, when set, indicates that a CRC error occurred in the data field during a read operation, or the error occurred in the header if a Read Header command was issued.

12 HEADER NOT FOUND—This bit, when set, indicates that the controller was unable to verify head position. This bit is reset by the Init or Reset functions.

13 NONEXISTENT MEMORY—When set, this bit indicates that BYSYNC L was not received within the required time period during a DMA transfer.

14 DRIVE FAULT/SEEK ERROR—When set, this bit indicates either that an error condition was detected within the drive or that a seek was not completed within the required time period.

15 COMPOSITE ERROR—When set, this bit indicates that one or more of the error bits is set (bits 10-14). If bit 6 is set and an error occurs, the current operation will be terminated and the interrupt routine will be initiated.

BUS ADDRESS REGISTER (RLBA)
774 402

15 — 00
BUS ADDRESS

The address of RLBAE is 774 402. The bits of this register contain the bus address of data transferred during read, write, or write check operations. The register is incremented by two at the end of each transfer. If the system has extended memory, the RLBAE will overflow to the EX MEM bits (04, 05) of the RLCS to reflect the extended bus address. This read/write register is cleared by the Init or Reset functions.

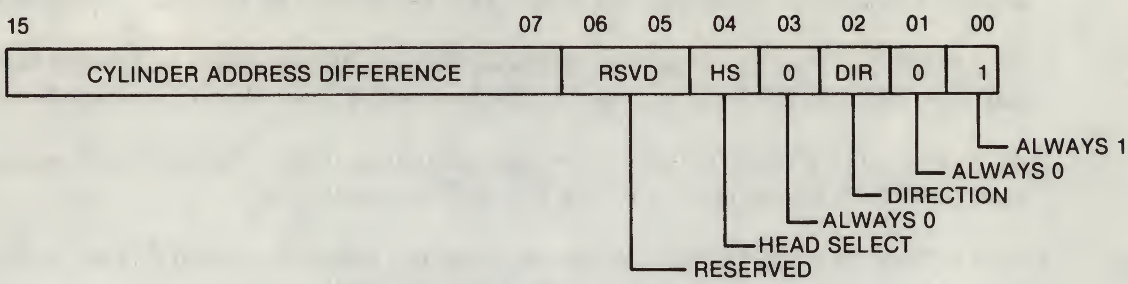
DISC ADDRESS REGISTER (RLDA) DURING READ/WRITE COMMANDS
(RL01/RL02 EMULATION)
774 404

15 — 07	06	05 — 00
CYLINDER ADDRESS	HA	SECTOR ADDRESS

HA — HEAD SELECT

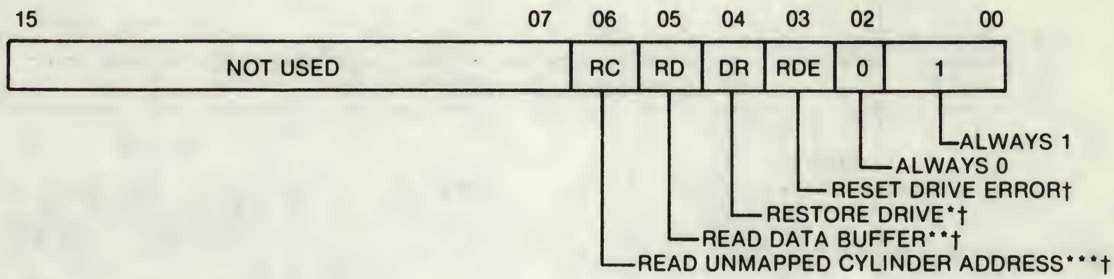
BIT(S)	DEFINITIONS
00-05	SECTOR ADDRESS—These six bits specify the sector address in octal.
06	HEAD SELECT—When set, this bit indicates that Head 1 is selected; when reset, Head 0 is selected.
07-15	CYLINDER ADDRESS—These nine bits specify the cylinder address in octal.

DISC ADDRESS REGISTER (RLDA) DURING SEEK COMMAND
774 404



BIT(S)	DEFINITIONS
00	ALWAYS 1
01	ALWAYS 0
02	DIRECTION—This bit indicates the direction in which a seek is to take place. When this bit is set, the heads move to a higher cylinder address. When this bit is cleared, the heads move to a lower cylinder address.
03	ALWAYS 0
04	HEAD SELECT—This bit indicates which head (disc surface) is to be selected. Set = Lower; Clear = Upper.
05-06	RESERVED
07-15	CYLINDER ADDRESS DIFFERENCE—This bit indicates, in octal, the number of cylinders the heads are to move on a seek.

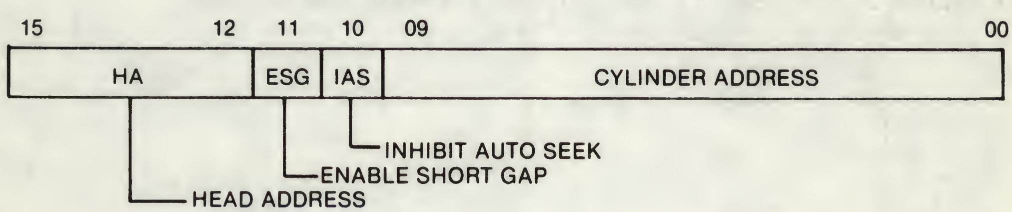
DISC ADDRESS REGISTER (RLDA) DURING A GET STATUS COMMAND
774 404



*Move Head to Cylinder Zero
**Read Data Buffer Using RLMP Register
***Allows Reading Real Disc Cylinder Address Using RLMP Register
†Get Status commands must be preceded by Controller Clear

BIT(S)	DEFINITIONS
00-01	ALWAYS 1
02	ALWAYS 0
03	RESET DRIVE ERROR—When this bit is set, the drive clears its error registers before sending a status word to the controller.
04	RESTORE DRIVE—When set, this bit will cause the heads to return to cylinder 0.
05	READ/WRITE DATA BUFFER—When this bit is set, reading from and writing to the Multipurpose register accesses the controller data buffer. Each successive access of the Multipurpose register increments the data buffer address.
06	READ UNMAPPED CYLINDER ADDRESS—When set, this bit causes the unmapped cylinder address to appear in the Multipurpose register.
07-15	NOT USED.

DISC ADDRESS REGISTER (RLDA) DURING FORMAT COMMANDS (BIT 15 OFF IN RLMP REGISTER)
774 404

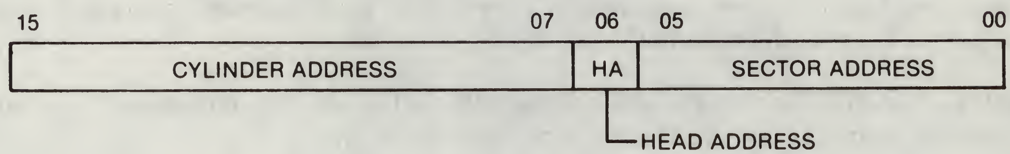


BIT(S)	DEFINITIONS
00-09	CYLINDER ADDRESS—These bits specify the address of the cylinder being accessed.
10	INHIBIT AUTO SEEK—When set, this bit inhibits Implied Seek.
11	ENABLE SHORT GAP—When set, this bit enables Short Gap.
12-15	HEAD ADDRESS—These bits specify the head address in octal.

MULTIPURPOSE REGISTER (RLMP) DURING READ/WRITE COMMANDS FOR WORD COUNT 774 406

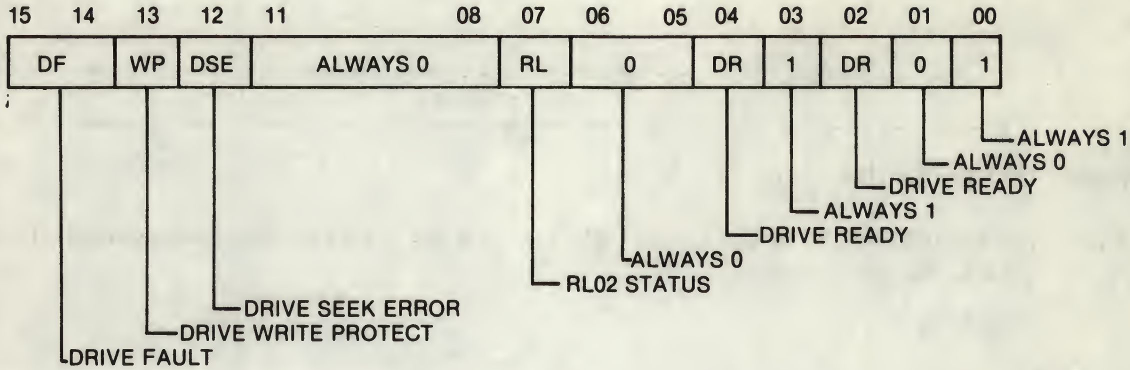
BIT(S)	DEFINITIONS
00-14	WORD COUNT—These bits are the 2's complement of the total number of words to be transferred during a read, write or write check operation. The register is incremented by one after each transfer. When the register overflows (all WC bits go to zero), the transfer is completed and the controller action is terminated at the end of the current disc sector.
15	DATA/FORMAT—When set, this bit indicates that data is read or written. When reset, this bit indicates that the format is read or written.

MULTIPURPOSE REGISTER (RLMP) DURING READ HEADER COMMAND 774 406



BIT(S)	DEFINITIONS
00-05	SECTOR ADDRESS—These bits indicate the addressed sector.
06	HEAD ADDRESS—This bit indicates the addressed head. Set = Lower; Clear = Upper.
07-15	CYLINDER ADDRESS—This bit indicates the addressed cylinder.

MULTIPURPOSE REGISTER (RLMP) DURING GET STATUS COMMAND
774 406



RLMP is used to read or write into the data buffer by using the Get Status command with bit 5 of RLDA. RLMP is also used to read the mapped cylinders and alternate cylinders with bit 6 of RLDA.

BIT(S)	DEFINITIONS
00	ALWAYS 1
01	ALWAYS 0
02, 04	DRIVE READY—When bits 02 and 04 are set, the drive is ready for operation.
03	ALWAYS 1
05-06	ALWAYS 0
07	RL02 STATUS—When set, this bit indicates that the drive is RL02; when cleared, the drive is RL01.
08-11	ALWAYS 0
12	DRIVE SEEK ERROR—When set, this bit indicates a seek error on the drive.
13	DRIVE WRITE PROTECT—When set, this bit indicates that the WRITE PROTECT switch has been set.
14-15	DRIVE FAULT—These bits set if an error condition is detected within the drive and is prohibiting all operations. These bits are reset manually by clearing the fault condition within the drive.

MULTIPURPOSE REGISTER (RLMP) DURING READ DATA BUFFER
774 406

15 — 00
DATA BUFFER

BIT(S) DEFINITIONS

00-15 DATA BUFFER—When bit 5 of RLDA is set during a Get Status command, the contents of the data buffer are displayed.

MULTIPURPOSE REGISTER (RLMP) DURING READ UNMAPPED CYLINDER COMMAND
774 406

15 — 10	09 — 00
NOT USED	CYLINDER ADDRESS

BIT(S) DEFINITIONS

00-15 CYLINDER ADDRESS—These bits list the cylinder address in binary.

ADDRESS EXTENSION REGISTER (RLBAE)
774 410

15 — 06	05 — 00
ALWAYS 0	ADDRESS EXTENSION BITS 21-16

The Address Extension register has the bus address 774 410. The purpose of this register is to hold the extra memory address bits not held in the RLBA.

BIT(S) DEFINITIONS

00-05 These bits, when set, define bits 16 through 21 of the Bus Address register.

06-15 ALWAYS 0

SECTION 5
TROUBLESHOOTING AND THEORY

This section describes troubleshooting procedures at three levels of complexity: basic system, controller symptoms and detailed analysis. Basic system troubleshooting procedures are visual checks not requiring test equipment and may be performed by the operator. Controller symptom procedures may require a scope, meter, extender board or diagnostics and should be performed by a technician. Detailed analysis is troubleshooting at the IC level, and is presented for engineers or system analysts for controller evaluation. The latter method may require the use of test equipment and the material presented here: board layout, term listing, theory of operation and logic diagrams.

CAUTION

Any troubleshooting requires a familiarity with the installation and operation procedures in this manual, the appropriate DEC manual, and the disc drive manufacturer's manual. Ensure power is off when connecting or disconnecting board or plugs.

BASIC SYSTEM TROUBLESHOOTING

The following should be checked before power is applied:

1. Verify that all signal and power cables are properly connected. Ribbon cable connectors are *not* keyed. The arrows on the connectors should be properly aligned.
2. Verify that all switches are properly set as described in Sections 2 and 3.
3. Verify that all modules are properly seated in the computer and are properly oriented.

The following should be checked during or after application of power:

1. Verify that the computer and disc drive generate the proper responses when the system is powered up.
2. Verify that the computer panel switches are set correctly.
3. Verify that the console can be operated in the local mode. If not, the console may be defective.
4. With the drive POWER switch on, verify that the drive READY light is on.
5. Verify that the green diagnostic light on the controller is on.

CONTROLLER SYMPTOMS

Controller symptoms, possible causes and checks/corrective action are described in Table 5-1. Voltage checks should be performed before troubleshooting more complex problems. The +12V and −5V sources are shown on Logic Diagram Sheet 20. The +5V source may be checked from any component shown on the other logic diagrams.

PHYSICAL LAYOUT

The physical layout of the board is shown in Figure 5-1. Column and row numbers on the layout correspond to the numbers of each IC on the logic diagrams.

TERM LISTING

The input and output terms for each logic diagram are described in Table 5-2. The sources and destinations refer to the sheet numbers of the logic diagrams.

Table 5-1. Controller Symptoms

Symptom	Possible Causes	Check/Corrective Action
1. Green diagnostic light on the controller is OFF.	1. Microprocessor section of controller inoperative: a. Bad oscillator b. Short or open on board c. Bad IC d. PROMs not properly seated	1. Controller/Place controller on extender board. With a scope, check the pins on the 2901. All pins except power and ground should be switching. Check for "stuck high" or "stuck low," or half-amplitude pulses. Check + 12V and − 5V power and + 5V at various IC's. Check PROMs A1 through A7 for proper seating. Check oscillator.
2. No communication between console and computer.	2. I/O section of controller "hanging" Q Bus: a. $\overline{\text{DEN}}$ always low b. Shorted bus transceiver IC. c. Bad CPU board.	2. Computer interface logic of controller/ a. Check signal $\overline{\text{DEN}}$ for constant assertion. b. Check I/O IC's. Remove controller board to see if trouble goes away. (Ensure slot is filled or jumpered.) c. Run CPU diagnostics.
3. No data transfers to/from disc.	3. Disc not ready, bad connection, or bad IC in register section of the controller.	3. Disc/Consult the disc manufacturer's manual for proper setting of disc switches, or READY, NO FAULT, or UNSAFE lights. Check cable connections. Controller Registers/Using ODT, examine the Drive Status Register. The DISC READY and SELECTED must be "one's." Using ODT, deposit "ones" and "zeros" in the remaining disc registers and verify proper register data.
4. Data transferred to/from from disc incorrect.	4. Multiple Causes: a. Bad memory in backplane b. Noise or intermittent source of DC power in computer. c. Bad IC in disc I/O section of controller. d. Bad area on disc. e. Disc heads not properly aligned.	4. Computer-controller-disc/ a. Run memory diagnostics. b. Check AC and DC power. c. While operating, check lines from controller to disc with a scope for short or open. d. Run the Format and Diagnostic Test program (Section 3). If errors occur at the same place on the disc, it is probably a bad area on the disc. Assign alternate tracks as specified in Section 3. e. Consult disc drive manufacturer's manual and align heads.
5. Intermittent failure—Controller runs for a short time after power is applied and then fails.	5. Failure of heat sense component on controller.	5. Isolate the bad component by using heat and cooling methods (heat gun, freon spray) and replace the bad component.

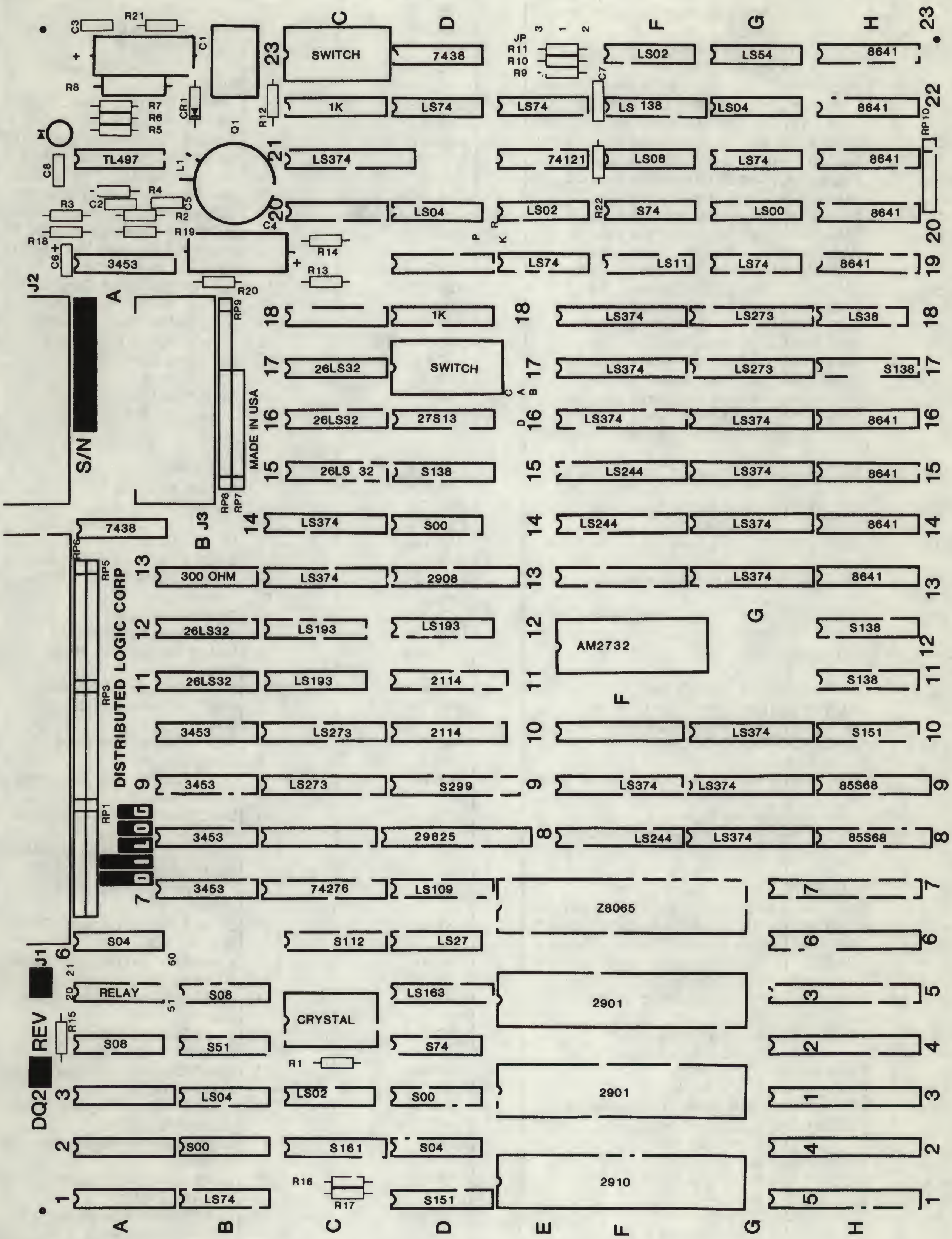


Figure 5-1. Board Layout

Table 5-2. Term Listing

Term	Origin	Description
AMF	17	Address Mark Found From Disc
BA00-BA09 +	15	Buffer Address Counter Bits 00-09
BBS7L	BUS (AP2)	Bus Peripheral Address Select
BBS7 +	4	Peripheral Address Select
BC4 +	13	Bit Count 4 From Bit Counter
BDAL00L	BUS (AW2)	Bus Data/Address Line 00
BDAL01L	BUS (AV2)	Bus Data/Address Line 01
BDAL02L	BUS (BE2)	Bus Data/Address Line 02
BDAL03L	BUS (BF2)	Bus Data/Address Line 03
BDAL04L	BUS (BH2)	Bus Data/Address Line 04
BDAL05L	BUS (BI2)	Bus Data/Address Line 05
BDAL06L	BUS (BK2)	Bus Data/Address Line 06
BDAL07L	BUS (BL2)	Bus Data/Address Line 07
BDAL08L	BUS (BM2)	Bus Data/Address Line 08
BDAL09L	BUS (BN2)	Bus Data/Address Line 09
BDAL10L	BUS (BP2)	Bus Data/Address Line 10
BDAL11L	BUS (BR2)	Bus Data/Address Line 11
BDAL12L	BUS (BS2)	Bus Data/Address Line 12
BDAL13L	BUS (BT2)	Bus Data/Address Line 13
BDAL14L	BUS (BU2)	Bus Data/Address Line 14
BDAL15L	BUS (BY2)	Bus Data/Address Line 15
BDAL16L	BUS (AC1)	Bus Address Extension Line 16
BDAL17L	BUS (AD1)	Bus Address Extension Line 17
BDAL18L	BUS (BC1)	Bus Address Extension Line 18
BDAL19L	BUS (BD1)	Bus Address Extension Line 19
BDAL20L	BUS (BE1)	Bus Address Extension Line 20
BDAL21L	BUS (BF1)	Bus Address Extension Line 21
BDINL	BUS (AH2)	Bus Data In
BDIN +	4	Data In
BDMGIL	BUS (AR2)	Bus DMA Grant In
BDGOL	BUS (AS2)	Bus DMA Grant Out
BDMRL	BUS (AN1)	Bus DMA Request
BDOUTL	BUS (AE2)	Bus Data Out
BDOUT +	4	Data Out
BEVENT	BUS (BR1)	Real Time Clock Control
BFULE +	3	Enable Buffer Full
BFULL –	15	Buffer Full
BIAKIL	BUS (AM2)	Bus Interrupt Acknowledge In
BIAKOL	BUS (AN2)	Bus Interrupt Acknowledge Out
BINITL	BUS (AT2)	Bus Initialize—Clear
BIRQ4L	BUS (AL2)	Bus Interrupt Request Level 4
BIRQ5L	BUS (AA1)	Bus Interrupt Request Level 5
BIRQ6L	BUS (AB1)	Bus Interrupt Request Level 6
BIRQ7L	BUS (BP1)	Bus Interrupt Request Level 7
BIT0-BIT10	16	Control Bits to Disc Drives
BIT7 + , –	13	"Complete Byte" Output of Bit Counter
BPOK-H	BUS (BB1)	Primary Power O.K.
BPOK –	4	Primary Power O.K.
BRPLYL	BUS (AF2)	Q Bus Reply
BRPLY +	4	Q Bus Reply
BSACKL	BUS (BN1)	DMA Select Acknowledge
BSYNCL	BUS (AJ2)	Bus Synchronize I/O
BTSPF +	2	Bootstrap Flag
BWTBTL	BUS (AK2)	Bus Write Byte
BWTBT +	4	Bus Write Byte
BYTCK +	13	Byte Clock
COUT +	10	Carry Out
CP1	12	Control Pulse 1
CP2	12	Control Pulse 2
CP3	12	Control Pulse 3
CP4	12	Control Pulse 4

Table 5-2. Term Listing (Continued)

Term	Origin	Description
CP5	12	Control Pulse 5
CP6	12	Control Pulse 6
CP7	12	Control Pulse 7
CRCER +	13	Cyclic Redundancy Check Error
CR1-0/7	9	Control Register One Bits 0-7
CR2-0/7	9	Control Register Two Bits 0-7
CR3-0/7	9	Control Register Three Bits 0-7
CR4-0/7	9	Control Register Four Bits 0-7
CR5-0/7	9	Control Register Five Bits 0-7
CR6-0/7	9	Control Register Six Bits 0-7
CSA0 + /CSA9 +	8	Control Store Address Bits 0-9
DA16 +	3	Extended Data/Address Bit 16
DA17 +	3	Extended Data/Address Bit 17
DAT0 + /DAT7 +	14,15	Data Buffer Bits 0-7
DBWC1 +	13	Data Buffer Write Control In
DBWS –	13	Data Buffer Write Strobe
DBWS1 –	13	Data Buffer Write Strobe In
DB00 + /DB07 +	6	Data Bus Bits 0-7
DB08 + /DB15 +	7	Data Bus Bits 8-15
DEN –	6	Data Enable
DMGI +	4	DMA Grant In
D00 + /D07 +	2,3,4,9,11, 12,14,17, 18,19	D-Bus Bits 0-7
EADD +	3	Enable Address
EADD –	6	Enable Address
EBITC +	3	Enable Bit Count
ECCO +	19	Error Correction Code Out
EDATA +	3	Enable Data
ENRD –	13	Enable Read Data Register
ENWD –	13	Enable Write Data To Buffer
FAULT	17	Drive Fault
GDATA +	13	Gated Read Data
GSCLK –	3	Gated System Clock
GTIRQ +	5	Gated Transmit Interrupt Request
IAKI +	4	Interrupt Acknowledge In
IAKIG –	2	Interrupt Acknowledge In Grant
INDEX	17	Index Pulse From Drive
INIT +	4	Initialize
LXR0 –	11	Load External Register Data Out MSB
LXR1 –	11	Load External Register Data Out LSB
LXR2 –	11	Load External Register DMA Address MSB
LXR3 –	11	Load External Register DMA Address LSB
LXR4 –	11	Load External Register Data Buffer LSB
LXR5 –	11	Load External Register Data Buffer MSB
LXR6 –	11	Load External Register Data Buffer
LXR7 –	11	Load External Register Extended Address
LXR9 –	11	Load External Register Drive Control Tags
LXRA –	11	Load External Register Drive Control Bus Bits
LXRB –	11	Load External Register Vector Address
LXRC –	11	Load External Register System Control
LXRD –	11	Load External Register Bootstrap Address
LXRE –	11	Load External Register CPU Bus Control

Table 5-2. Term Listing (Continued)

Term	Origin	Description
LXRF –	11	Load External Register RAM Destination
MRQB +	3	Memory Request Q Bus
OCD + / –	16	Open Cable Detect
ONCYL + / –	17	On Cylinder From Drive
PICK	16	Power Pick
QBUSA	2	Q Bus Access
Q3	10	Q Register Shift Line
RAM3 +	10	Shift Output of ALU RAM
RCLOCKA/B + / –	18	Read Clock From Drives A or B
RDATAA/B + / –	18	Read Data From Drives A or B
RDATA +	18	Read Data
REP	19	Read Error Pattern
RESET	4	Reset Signal to Controller
RMCLK	3	RAM Clock
RSYNC –	13	Read Synchronize
R/WCK –	18	Read/Write Clock
R/WSRE +	3	Read/Write Shift Register Enable
SELA/B	18	Drives A or B Selected
SENDA/B	18	Drives A or B Seek End
SCLK	3	System Clock
SCLOCKA/B	18	Servo Clock From Drives
SDB08 +	2	Slave Data Bus Bit 8
SEEKA/B	18	Seek End From Drives
SEC + / –	17	Sector Pulse From Drive
SERR + / –	17	Seek Error From Drives
SL/IN +	2	Slave Interrupt Acknowledge Request
TAG1/2/3	16	Tag Lines To Drives
TDIN +	3	Transmit Data In
TDOUT +	3	Transmit Data Out
TDMG +	2	Transmit Direct Memory Grant
TDMR +	2	Transmit Direct Memory Request
TIAK +	2	Transmit Interrupt Acknowledge
TIRQ +	3	Transmit Interrupt Request
TRPLY	3	Transmit Reply
TSACK	2	Transmit Select Acknowledge

Table 5-2. Term Listing (Continued)

Term	Origin	Description
TSYNC	3	Transmit Synchronize
TWTBT	3	Transmit Write Byte
UNRDY	17	Drive Unit Ready
USEL0/1/2/3	16	Drive Unit Select Bits 0, 1, 2, 3
USELA/B	18	Drive Unit Select A, B
USTAG	16	Drive Unit Select Tag
VEC –	8	Vector Address Register Select
WDATA +	14	Write Data Bit Stream
WCLOCKA/B + / –	18	Write Clock To Drives A or B
WDATAA/B + / –	18	Write Data To Drives A or B
WPRT	17	Drive Write Protect
WREN –	3	Write Enable
XSD0	11	External Source Decode Slave Address
XSD1	11	External Source Decode Data Input MSB
XSD2	11	External Source Decode Data Input LSB
XSD3	11	External Source Decode CPU Bus Status
XSD4	11	External Source Decode Data Buffer
XSD5	11	External Source Decode Disc Drive Status
XSD6	11	External Source Decode Seek End Status
XSD7	11	External Source Decode Error Status Register
XSD8	11	External Source Decode Bootstrap PROM
XSD9	11	External Source Decode Configuration Switches
XSDA	11	External Source Decode Literal PROM
XSDB	11	External Source Decode RK06 Switches
XSDF	11	External Source Decode RAM
Y00/Y07	10	Y-Bus Bits 0-7
ZERO +	10	Zero Output of 2901
1K0V +	15	1024 Address Counter Overflow

THEORY

The controller may be examined as three parts: computer interface, disc interface and controller internal functions. Signals from and to the computer are described in Section 1, Table 1-1. Signals from and to the disc drive are described in Tables 1-2 and 1-3. Figure 5-2 is a simplified block diagram illustrating the interfaces and some of the functional components. Single lines in the illustration represent serial data and the wider lines represent parallel data. A detailed block diagram of the controllers is shown on Sheet 1 of the logic drawings. The number in the blocks on Sheet 1 refer to the sheet numbers of the other logic diagrams.

Computer Interface

The purpose of the computer interface is to (1) buffer lines between the Q Bus of the LSI-11 computer and the controller, and (2) to synchronize information transfers. The controller is a slave device during initialization and status-transfer sequences. The controller is selected by base address 777 440_8. The controller is bus master during data transfers and either receives data from or outputs data to the computer memory via the LSI-11 DMA facility.

The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are unidirectional and used for "bus arbitration." Bus synchronization is fully controlled by the controller microprocessor. This allows the computer bus to be used by other devices when the disc controller is busy with internal functions and controller/disc data transfers.

Data bus driver/receiver registers 13H through 16H (Sheets 6 and 7) buffer the input data and distribute it as DB 00-15 in the controller. The DB

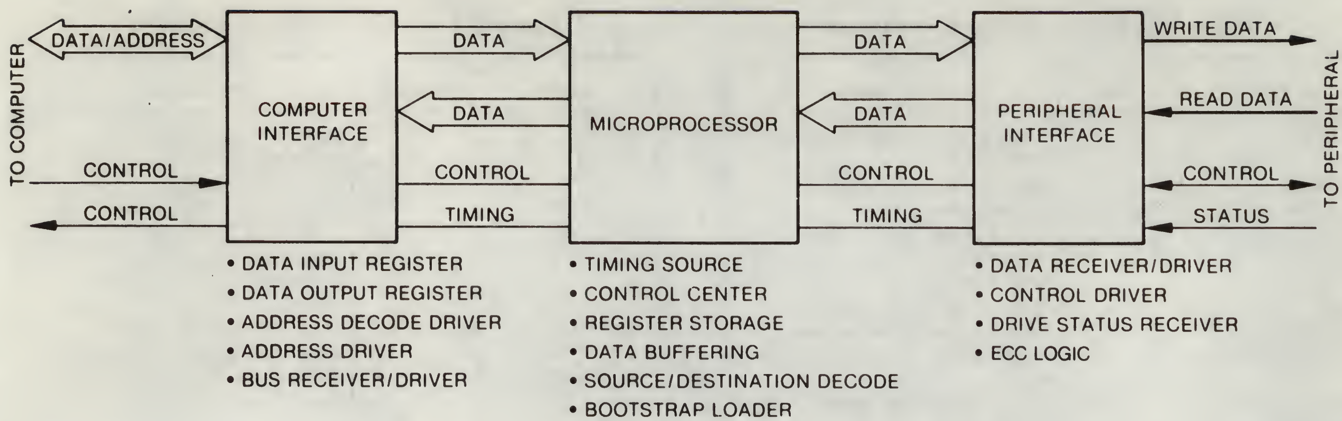


Figure 5-2. Simplified Block Diagram

signals are routed to a data input multiplexer (MUX) and address decode registers located on Sheets 12 and 2.

Output data and addresses from the microprocessor Y Bus (Y00-Y07) are latched by registers 13G through 16G, and transferred to the Q Bus via bus driver/receivers 13H through 16H (Sheets 6 and 7).

Note that the Device Enable signal (DEN−) is active when either the Address Enable (EADD) or the Data Enable (EDATA) signal is active. DEN controls the operating mode of all data and address driver/receivers, under control of the firmware, via the Y Bus (Sheets 6 and 7).

Disc Interface

The disc is connected to the controller by separate data and control cables. A common control cable is daisy chained to both drives in a multiple-drive configuration, while separate data cables are always used.

Serial read data is received by receivers 16C or 15C (Sheet 18) and then converted to parallel data by the read/write shift register 9D (Sheet 14). In the reverse direction, parallel data from the data buffer is converted to serial data by the shift register, then sent to data cable drivers (Sheet 18).

The control cable drivers 7B, 8B, 9B and 10B (Sheet 16) are always enabled and are driven by the output of registers 9C and 10C, which act as latches to capture the Y Bus data from the microprocessor.

Control cable receivers 11B and 12B (Sheet 17) supply data to the disc status register/multiplexer 13C (Sheet 17) at all times. The data is available to the microprocessor via the D Bus when signal XSD5− is active.

Controller Internal Functions

The microprocessor is the timing and control center of the controller. The microprocessor is controlled by instructions stored in Programmable Read Only Memory (PROM). The instructions, called "firmware," cause the microprocessor to operate in a prescribed manner during each of the computer-selected functions. These functions are established by a series of instructions issued by the LSI-11.

Because the disc and the computer transfer data at different rates, it is necessary to buffer data going to and from the disc. High-speed Random Access Memory (RAM) allows a full sector of data to be buffered during read and write operations.

All data transfer and computer/disc protocol is under microprocessor control. This feature allows modification of controller operating characteristics by making changes only to the firmware. Input/output logic remains essentially unchanged.

The output from the microprocessor is the Y Bus. Y-Bus instructions govern all controller operations by acting as the controller source for all receivers and drivers either directly or through the source/destinations decode IC's (Sheet 11).

The D Bus is the data input to the microprocessor. Tri-state drivers allow many signal sources to be connected to the bus while only one at a time is enabled by the source/desgination decode logic (Sheet 11).

The following list describes D-Bus enabling signals:

Function	Term	Component Enabled	Sheet
Slave Address	XSD0	16F	2
Data Input (MSB)	XSD1	14F	12
Data Input (LSB)	XSD2	15F	12
Q-Bus Status	XSD3	18F	12
Data Buffer	XSD4	8F	14
Disc Status	XSD5	13C	17
Seek End/Unit Select	XSD6	14C	18
Error Status	XSD7	9F	19
Boot PROM	XSD8	12F	11
Switches	XSD9	17F	3
Literal	XSDA	7H	9
RK06 Switches	XSDB	21C	5
Scratch RAM Enable	XSDF	8H, 9H	12

All data on the D Bus is under control of the firmware as decoded by source PROMs 11H, 15D on Sheet 11. The microprocessor selects the proper input data by enabling one of the above lines.

The Y Bus is the microprocessor output. Output of the microcode PROM 5H (Sheet 9) is decoded by 12H and 17H (Sheet 11) to select the destination of the data on the Y Bus.

The following list describes Y-Bus enabling signals:

Function	Term	Component Enabled	Sheet
Data Out Register (MSB)	LXR0	13G	7
Data Out Register (LSB)	LXR1	15G	6
DMA Address (MSB)	LXR2	14G	7
DMA Address (LSB)	LXR3	16G	6
Data Buffer Address (LSB)	LXR4	11C, 12D	15
Data Buffer Address (MSB)	LXR5	12C	15, 19
Data Buffer Load	LXR6	7C, 8G	13, 14
Load Extended Address	LXR7	13D	7
Drive Control (Tags)	LXR9	10C	16
Drive Control (Bus 0-7)	LXRA	9C	16
Load Vector Address	LXRB	10G	8
System Control	LXRC	18G	3
External Event	LXRD	22D	17
Q-Bus Control	LXRE	17G	3
RAM Destination	LXRF	8H, 9H	12

With the single exception of bus reply detector 21E (Sheet 3), all Y-Bus data and address activity is controlled by the 15 signals shown above.

Each LXR (Load External Register) signal activates a register which, in conjunction with Y-Bus data, latches the appropriate data word.

Control Registers CR1 through CR6 are the outputs of the microcode PROMs (Sheet 9). These signals control the microprocessor functions and provide the data to the source/destination decode logic (Sheet 11).

Data Buffer

The data buffer and associated logic are shown on Sheets 13, 14 and 15. Data transfers to and from the buffer are both two-step operations. First, an entire sector of data is loaded into the buffer during either a read or write operation. Once loaded, the buffer contents are then transferred to disc or LSI-11 memory in a completely separate operation. Figure 5-3 illustrates read and write operations to and from the RAM data buffer.

During a write operation, parallel data (Y00-Y07) is transferred from LSI-11 memory via microprocessor to the write data register 8G (Sheet 14). The data (DAT0-DAT7) is then transferred to the buffer 10D and 11D (Sheet 15). Parallel data (DAT0-DAT7) from the buffer is then transferred to shift register 9D, converted to serial data (W DATA), and transferred to the data cable driver 19A (Sheet 18).

During a read operation, Serial Read Data (R DATA) from the data cable receivers is ANDED with Enable Bit Count (E BIT C) resulting in the signal G DATA. This signal enters the shift register 9D and is transferred as parallel data to the read data register 8D, for transfer to the data buffer while the next byte is being shifted through shift register 9D. The read data from the buffer (DAT0-DAT7) is transferred to driver 8F (Sheet 14) to the microprocessor for transfer to LSI-11 memory.

The counter located at 11C, 12C and 12D (Sheet 15) is used to address the location in the buffer into which data can be written or read from. The counter can be preset to a specific starting address via the Y Bus of the microprocessor.

ERROR CORRECTION CODE (ECC) LOGIC

Functional Operation

The ECC Generator does not correct errors; it generates codes during write and read operations and during reading generates a syndrome. A syndrome is the result of merging check characters being read with check characters generated. A zero syndrome indicates no error; a nonzero syndrome indicates an error. This syndrome contains all the information necessary to find the error location and the error pattern, i.e., to allow error correction.

The error location is found by counting the number of clock pulses required to make the EP output go high. The error pattern is then available on the LP0-LP3 and Q0-Q7 outputs and can be used to exclusive OR with data. Depending upon the position of switch S5 (location D17), either the computer or the controller corrects the error. Note that some error patterns cannot be corrected. These are flagged to the computer.

Component Description

During a write operation a 32-bit ECC is appended to the header record and a 56-bit ECC is appended to the data record of each sector of information on the disc. ECCs are also generated while information is being read from the disc. The codes generated during the read operation are compared with the equivalent codes previously written. Discrepancies detected (errors) are signaled to the microprocessor and corrected if possible.

The ECC logic is shown on Sheet 19. The ECC Generated (7E), also referred to as the Burst Error

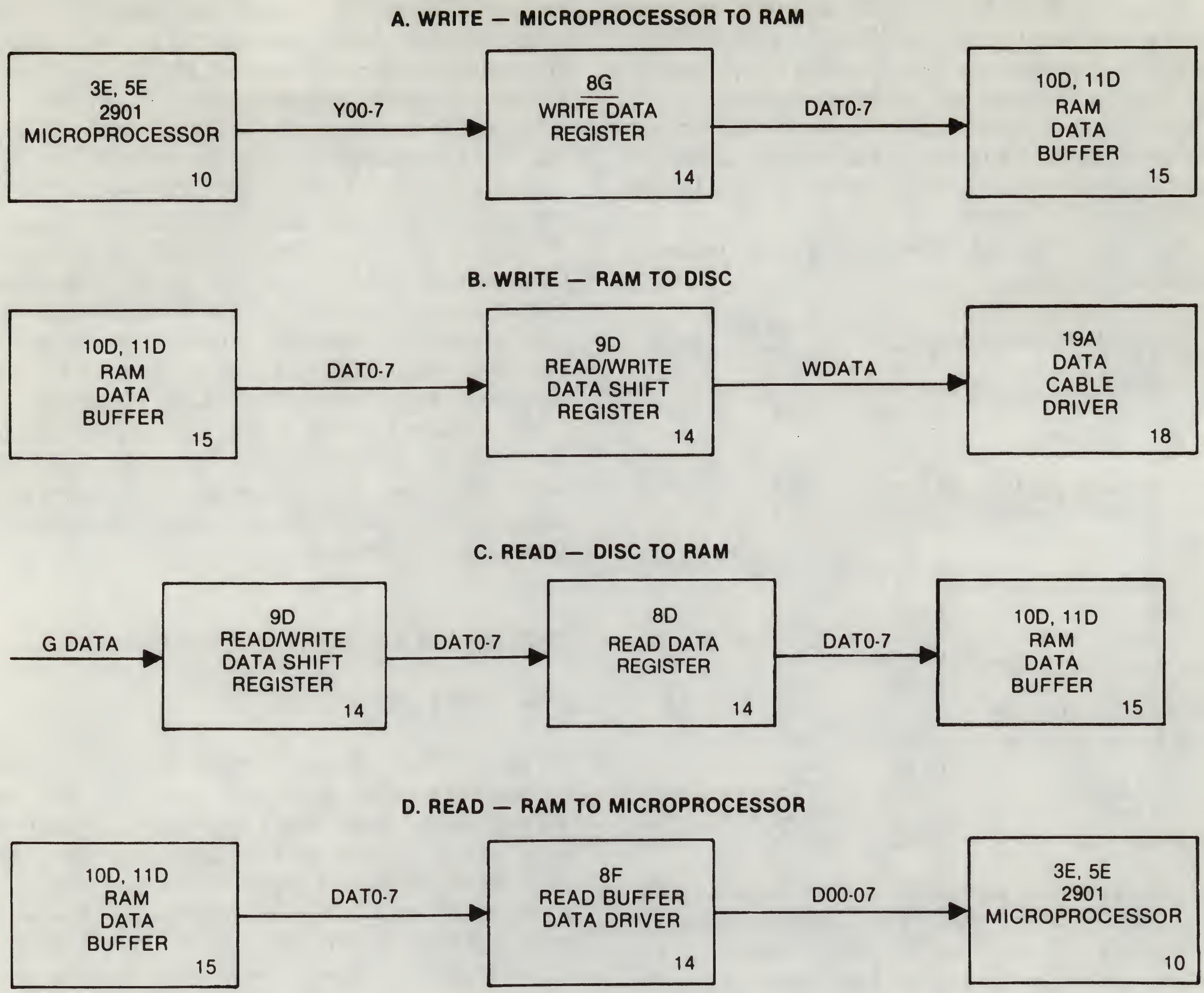


Figure 5-3. Data Paths

Processor, is used in three different types of operations: write, read, and correct. Detailed information about the ECC generator is given by an AMD, AM9520/Z8065 product specification.

During writing or reading, information is connected to the D0-D7 inputs of the ECC generator. Select inputs S0 and S1 to determine whether a 32- or 56-bit polynomial is being used. The 32-bit polynomial is used for ECC header checks, and the 56-bit polynomial is used for data record check. The Data Buffer Write Strobe (DBWS) is the source of Clock Pulses (CP) to the ECC generator.

Control information for the ECC generator from the Y Bus is stored by LXR5 into ECC Control register 9G.

When Master Reset (MR—) is asserted, the logic is initialized. Asserting REP (Read Error Pattern) makes outputs LP0-LP3 and Q0-Q7 active.

Control inputs P0-P3 are not used. The ECC generator functions selected by inputs C0-C2 are as follows:

C2	C1	C0	Function
L	L	L	Compute Check Bits
L	L	H	Write Check Bits
L	H	L	Read Normal
H	L	L	Load
H	H	L	Correct Normal

Check bit outputs Q0-Q7 are connected to the DAT0-DAT7 lines one byte at a time under control of REP and C0-C2. The remaining outputs of the ECC generator are stored in ECC status register 9F by Clock GSCLK. The microprocessor monitors ECC status on the D Bus during XSD7 time.

Outputs LP0-LP3 (Located Error Pattern), together with outputs Q0-Q7, provide the 12-bit

error pattern. Q7 is the MSB and LP0 is the LSB of the pattern. Outputs LP0-LP3 are active only when REP is asserted. Output AE (Alignment Exception) is asserted if the error pattern will not line up automatically during a correction sequence. This can occur because of the method of polynomial division implemented in the ECC generator.

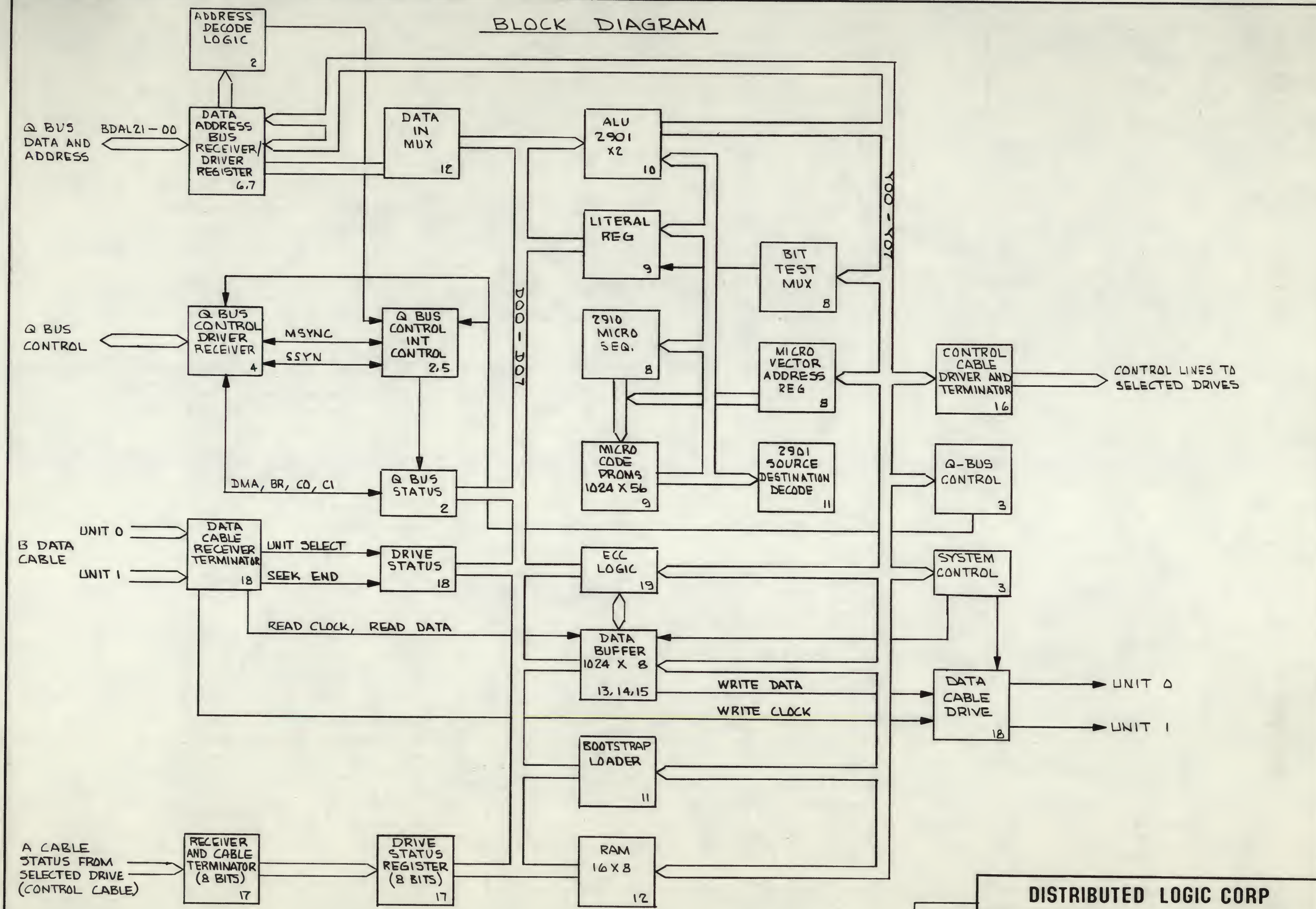
Output EP (Error Pattern) is asserted when the error pattern has been located during the correction sequence. Output ER is asserted if an error was detected after the last check byte had been read during a read function.

+12 VOLT TO −5 VOLT POWER SUPPLY

The +12 to −5 volt power supply shown on Sheet 20 is a dc-to-dc converter that produces the −5 volts required for the current mode line driver to the disc(s).

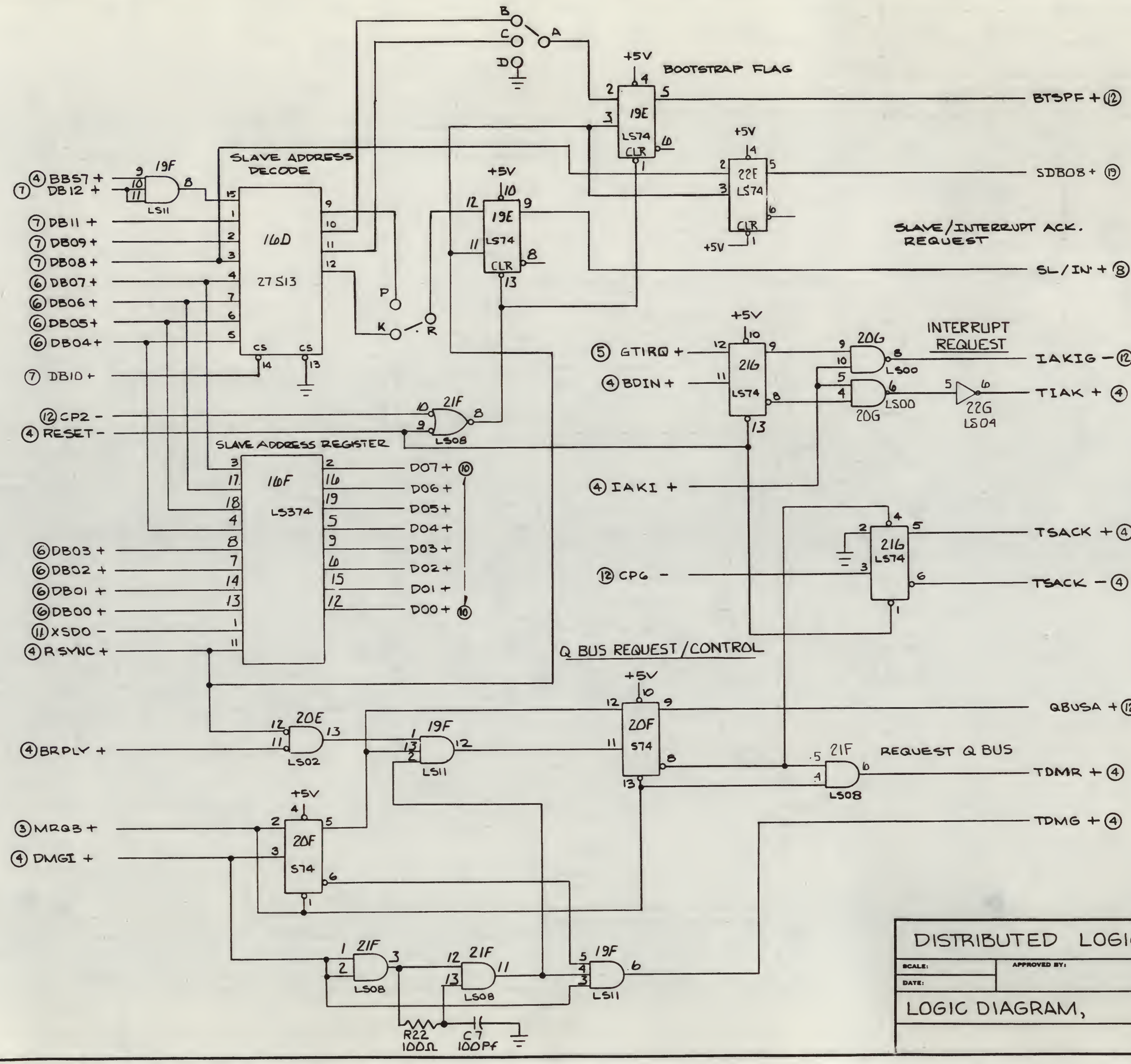
Input power is obtained from the +12 volts on the backplane. Oscillator R19, C6, 14A provides a rectangular pulse that drives current switch Q1. When the oscillator turns Q1 on, +12V is applied to L1 and an increasing current is produced. When the oscillator turns off Q1, the energy stored in L1 produces a negative voltage (at the top of L1), charging diodes C4 and C5 through diode CR1. Successive oscillator pulses cause the voltage across G5, G4 to build up to approximately −5 volts. Circuit 21A is a zener-referenced regulator that produces a threshold control voltage that regulates the duty cycle of the oscillator drive voltage applied to Q1 (increasing or decreasing "on" time). Circuit 21A thus controls the energy stored in L1 to maintain and regulate the voltage on G5, G4 at −5 volts under normal load conditions.

BLOCK DIAGRAM



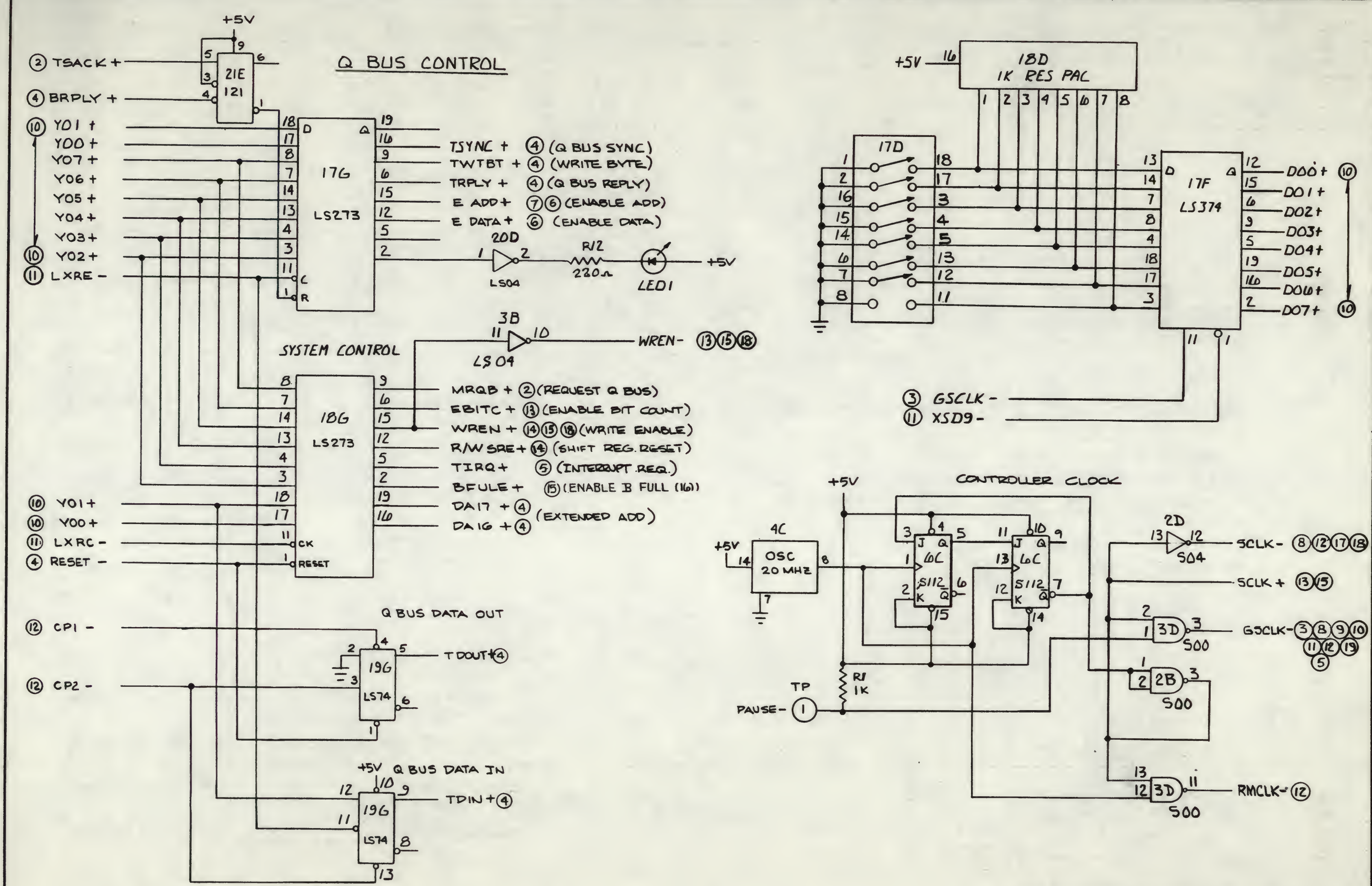
	DISTRIBUTED LOGIC CORP		
DQ228	SCALE: / DATE:	APPROVED BY:	DRAWN BY RQ / REVISED 7-14-83
DQ215	LOGIC DIAGRAM		
DQ214			
USED ON			DRAWING NUMBER 853027 B

17 X 22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 2 OF 20
		DRAWING NUMBER 853027 B

17X22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



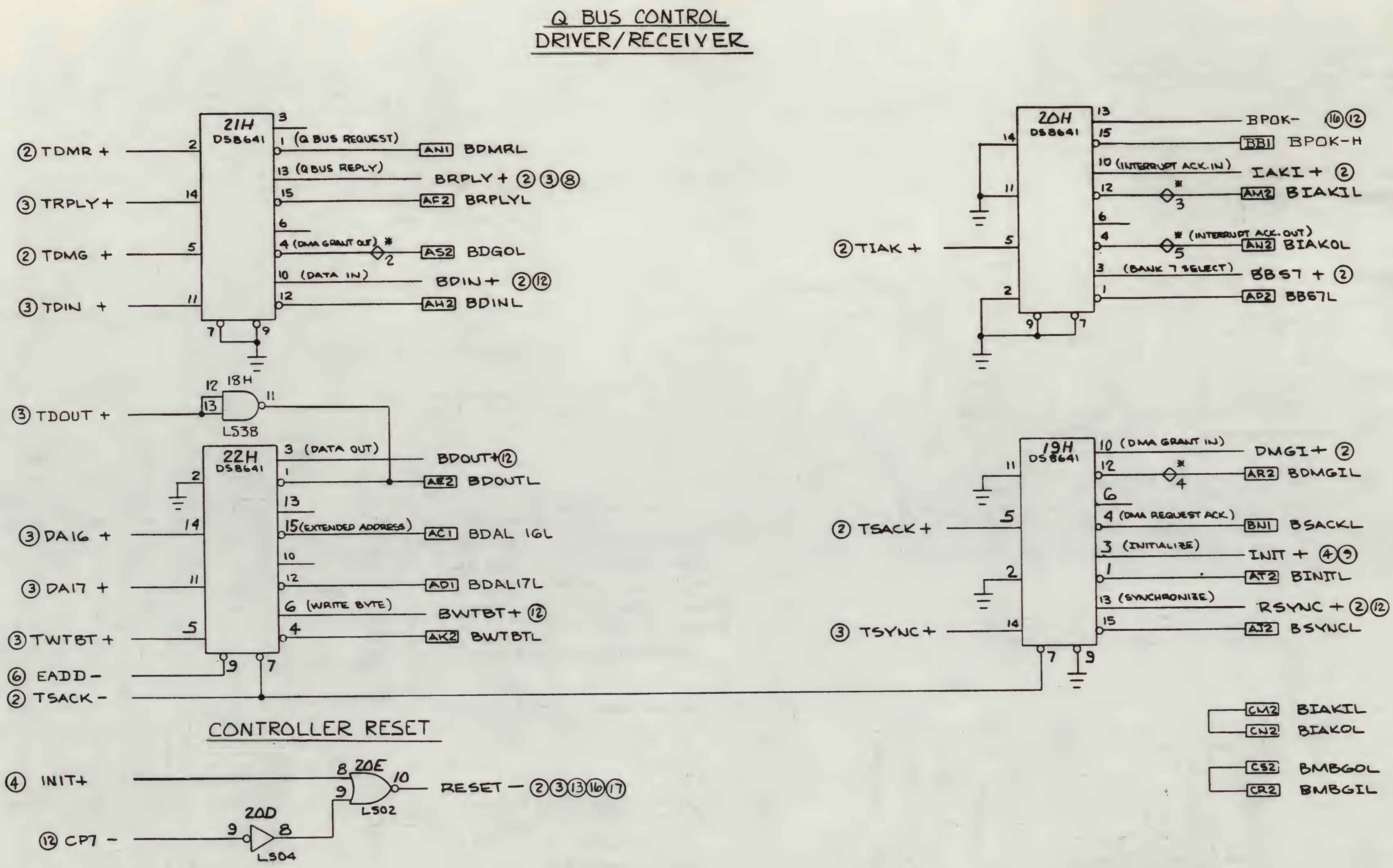
DISTRIBUTED LOGIC CORP.

SCALE: | DATE: | APPROVED BY: | DRAWN BY R.E. | REVISED

LOGIC DIAGRAM,

SHT 3 OF 20

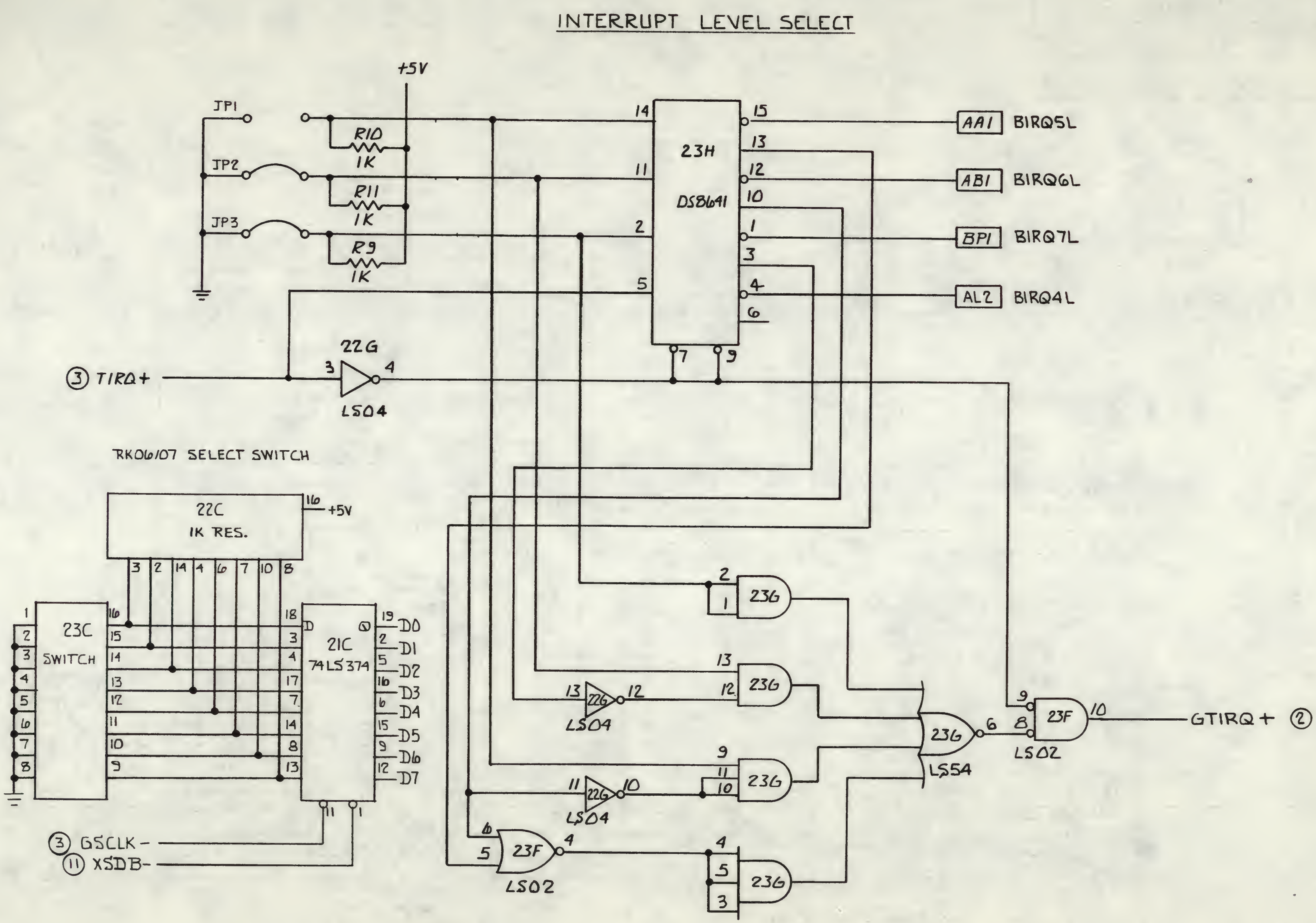
DRAWING NUMBER 853027 B



NOTE: * — 12 SYMBOL INDICATES PULL-UP (180Ω) / PULL-DOWN (390Ω) RESISTORS. NUMBER SHOWN IS PIN NUMBER USED IN PACK, LOCATION RP10.

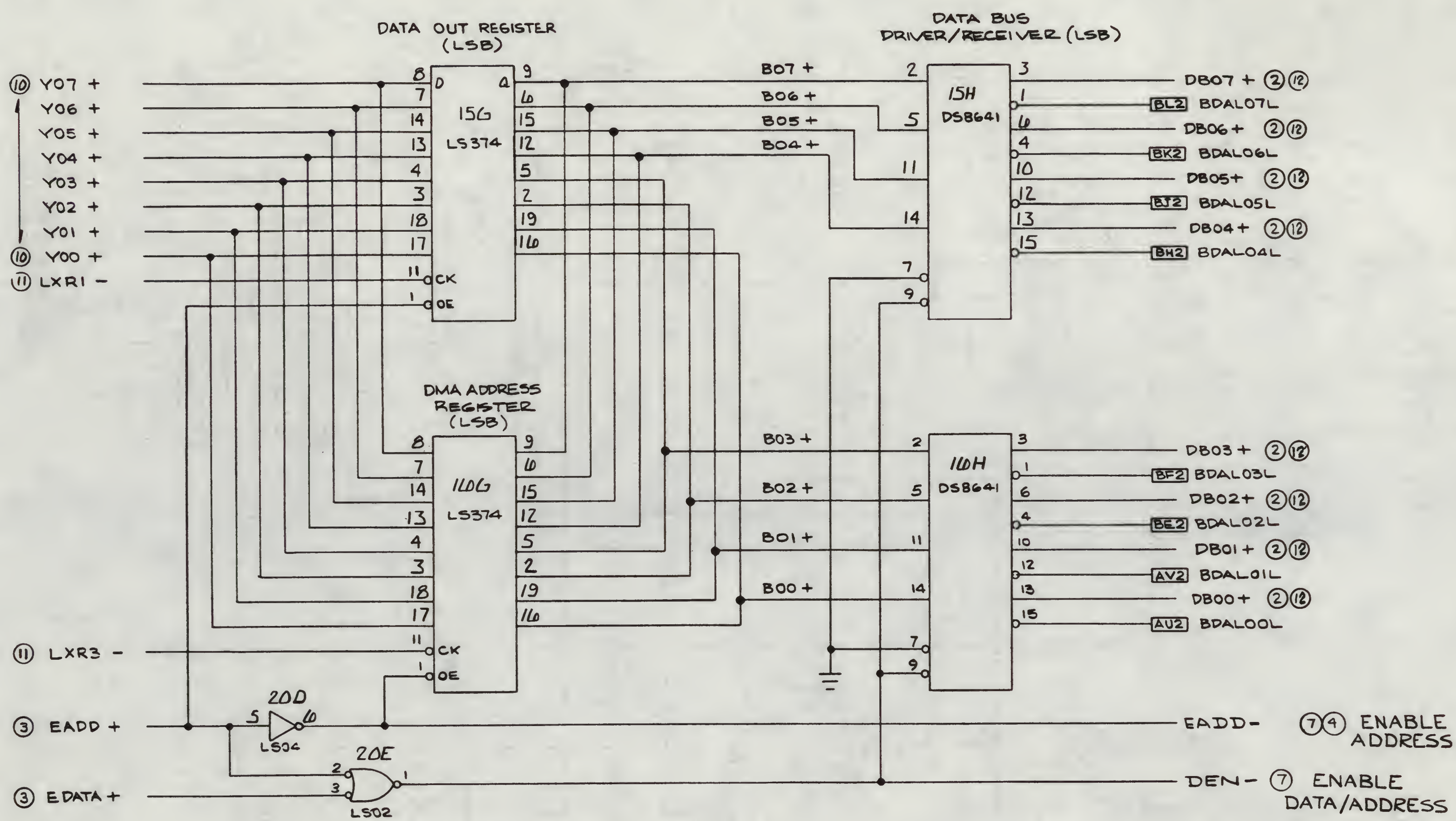
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM		SHT 4 OF 20
		DRAWING NUMBER 853027 B

17X22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



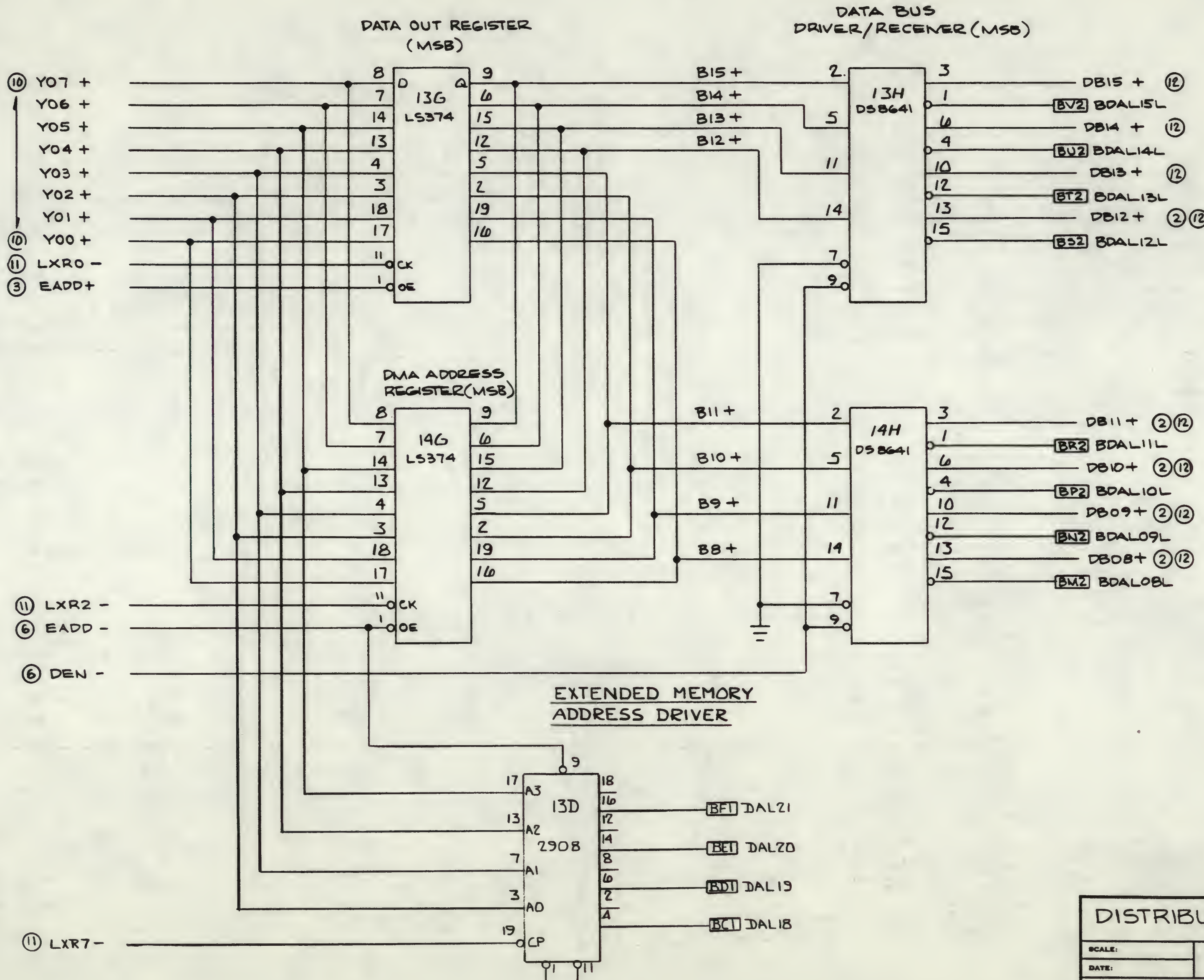
DISTRIBUTED LOGIC CORP.		
SCALE: / DATE:	APPROVED BY:	DRAWN BY R.E. / REVISED
LOGIC DIAGRAM		SHT 5 OF 20
		DRAWING NUMBER 853027 A

17X22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



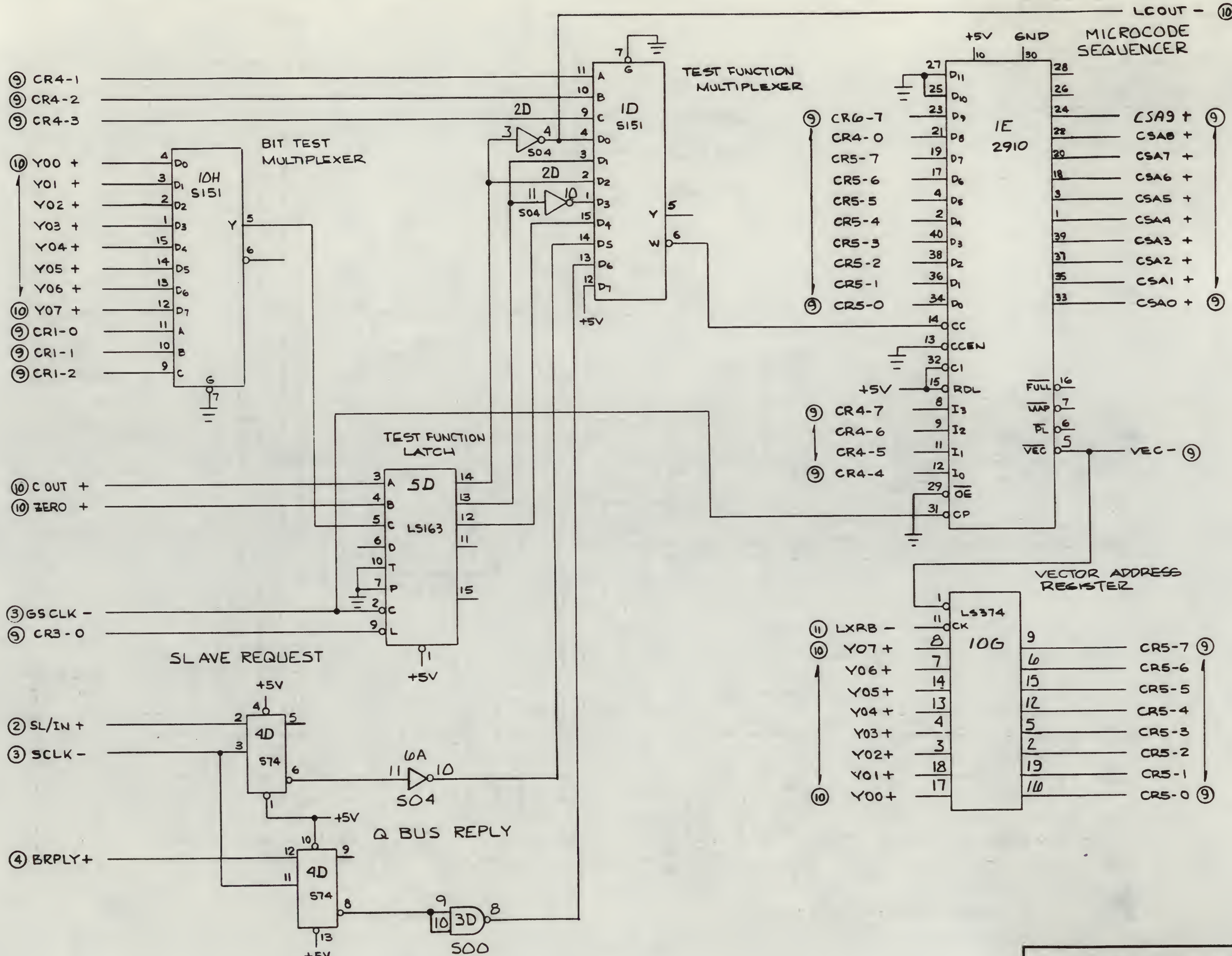
DISTRIBUTED LOGIC CORP.		
SCALE: / DATE:	APPROVED BY:	DRAWN BY R.E / REVISED
LOGIC DIAGRAM,		SHT 6 OF 20
		DRAWING NUMBER 853027 A

17X22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



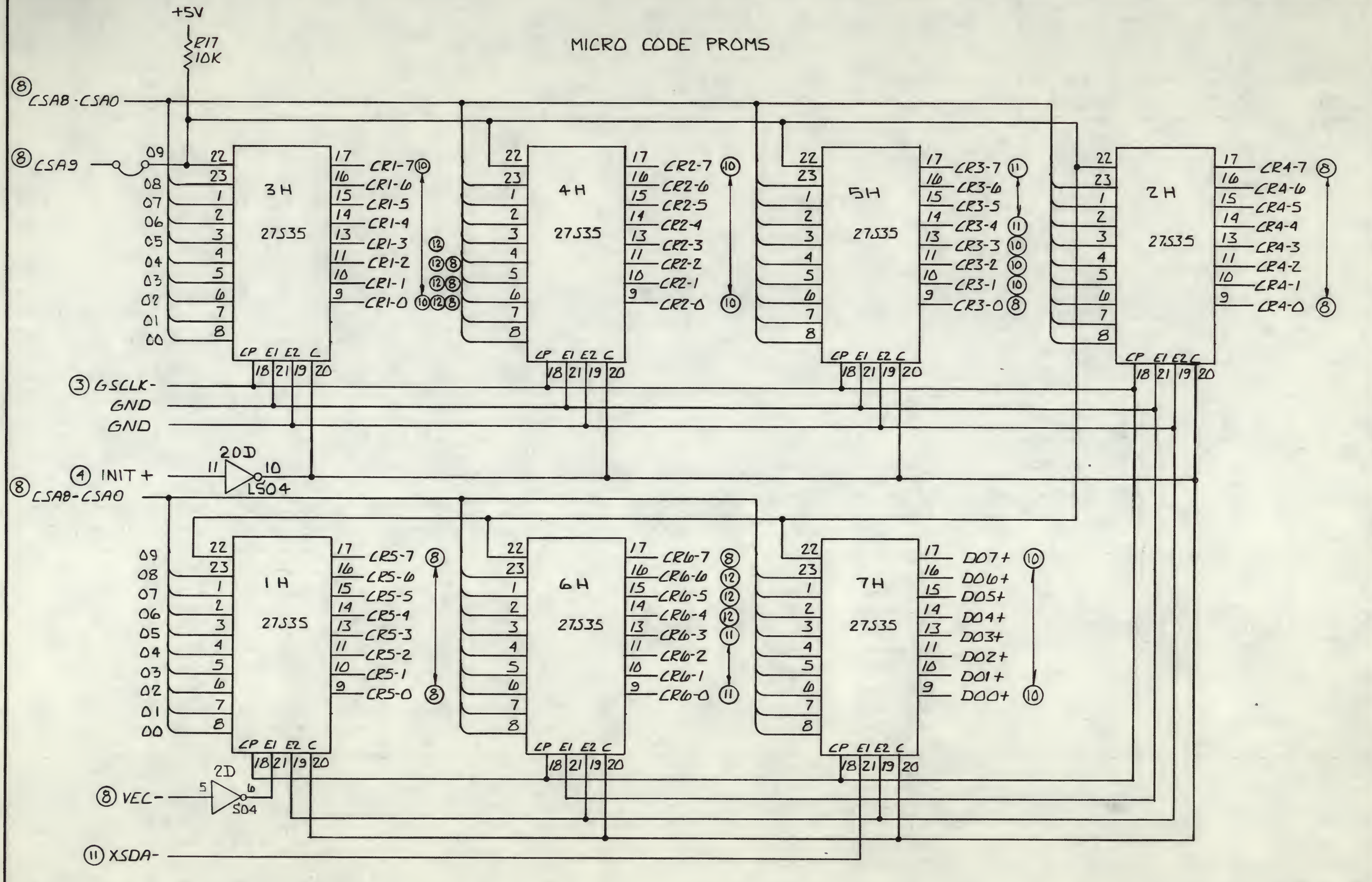
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 7 OF 20
		DRAWING NUMBER 853027 A

17X22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R. E.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 8 OF 20
		DRAWING NUMBER 853027 A

MICRO CODE PROMS



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM		SHT 9 OF 20
		DRAWING NUMBER 853027 A

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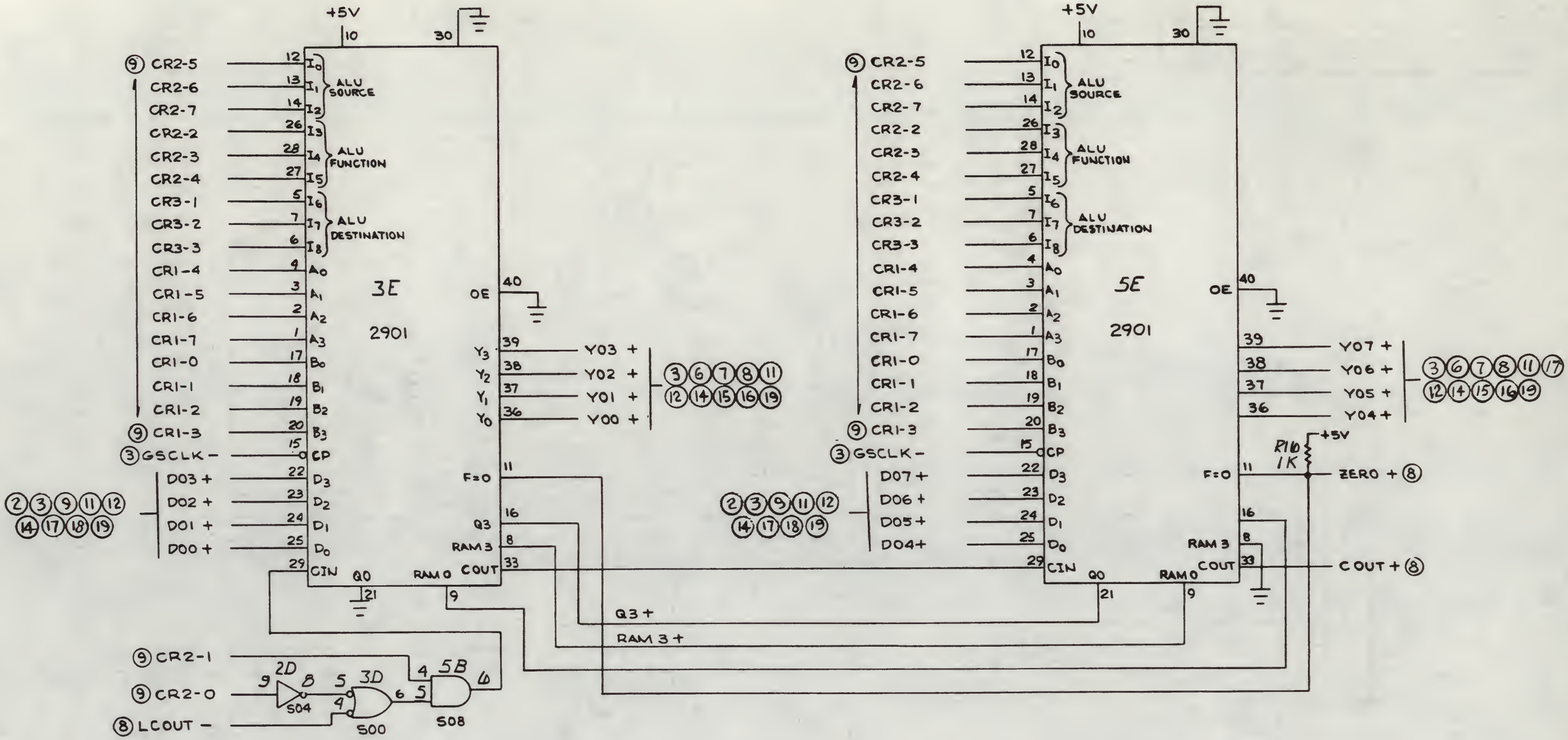

DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
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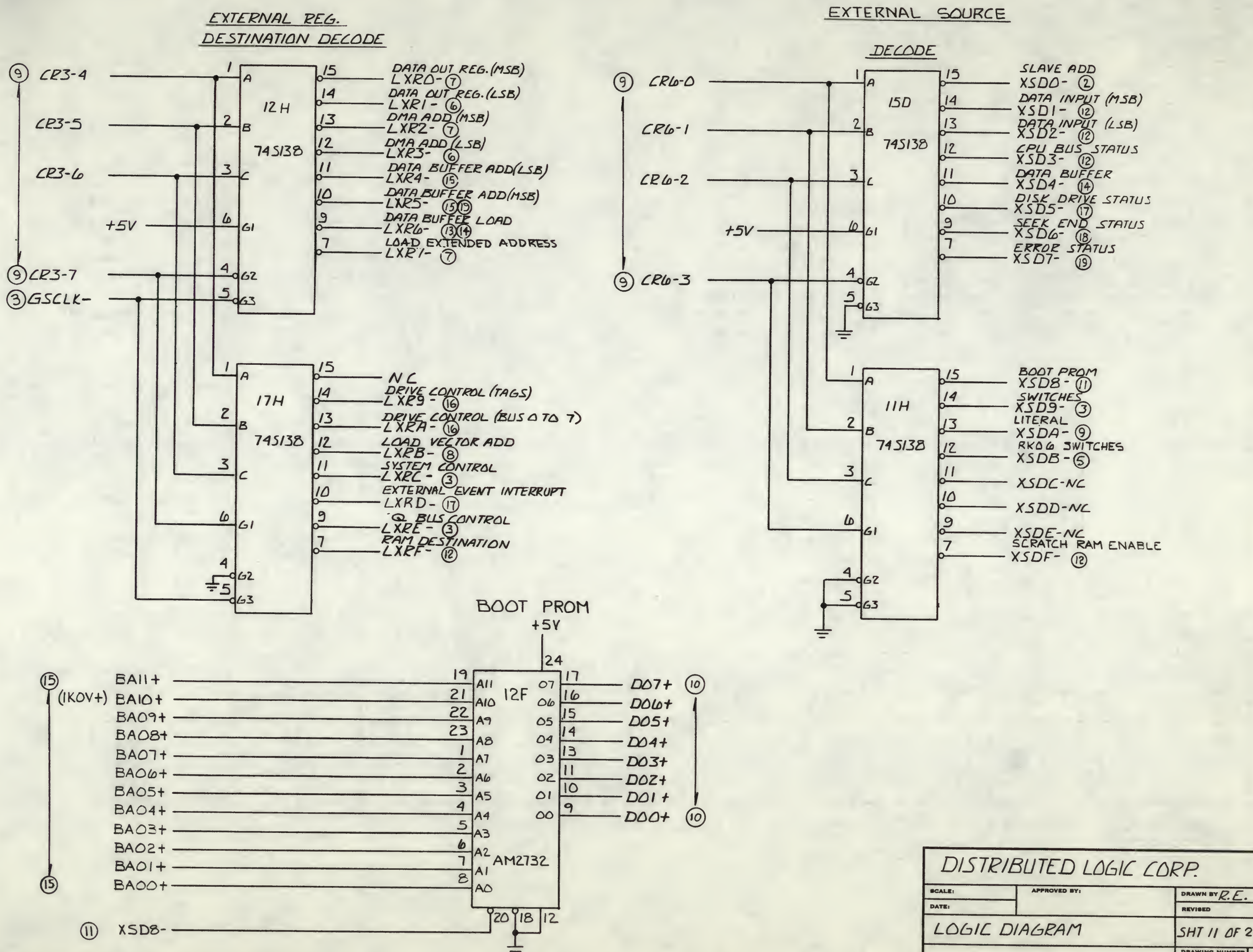
LOGIC DIAGRAM,		SHT 10 OF 20
		DRAWING NUMBER 853027 B

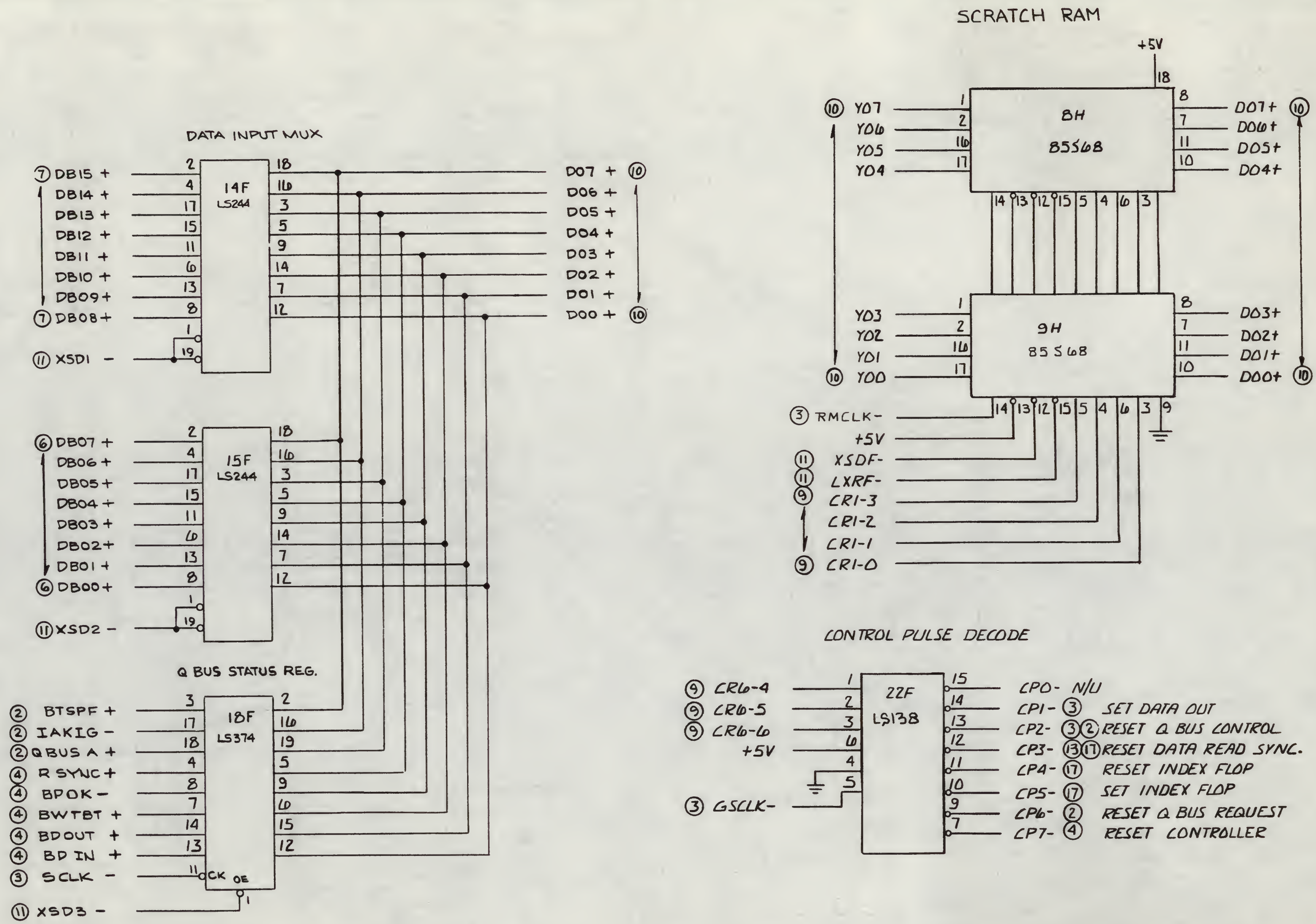
17X22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



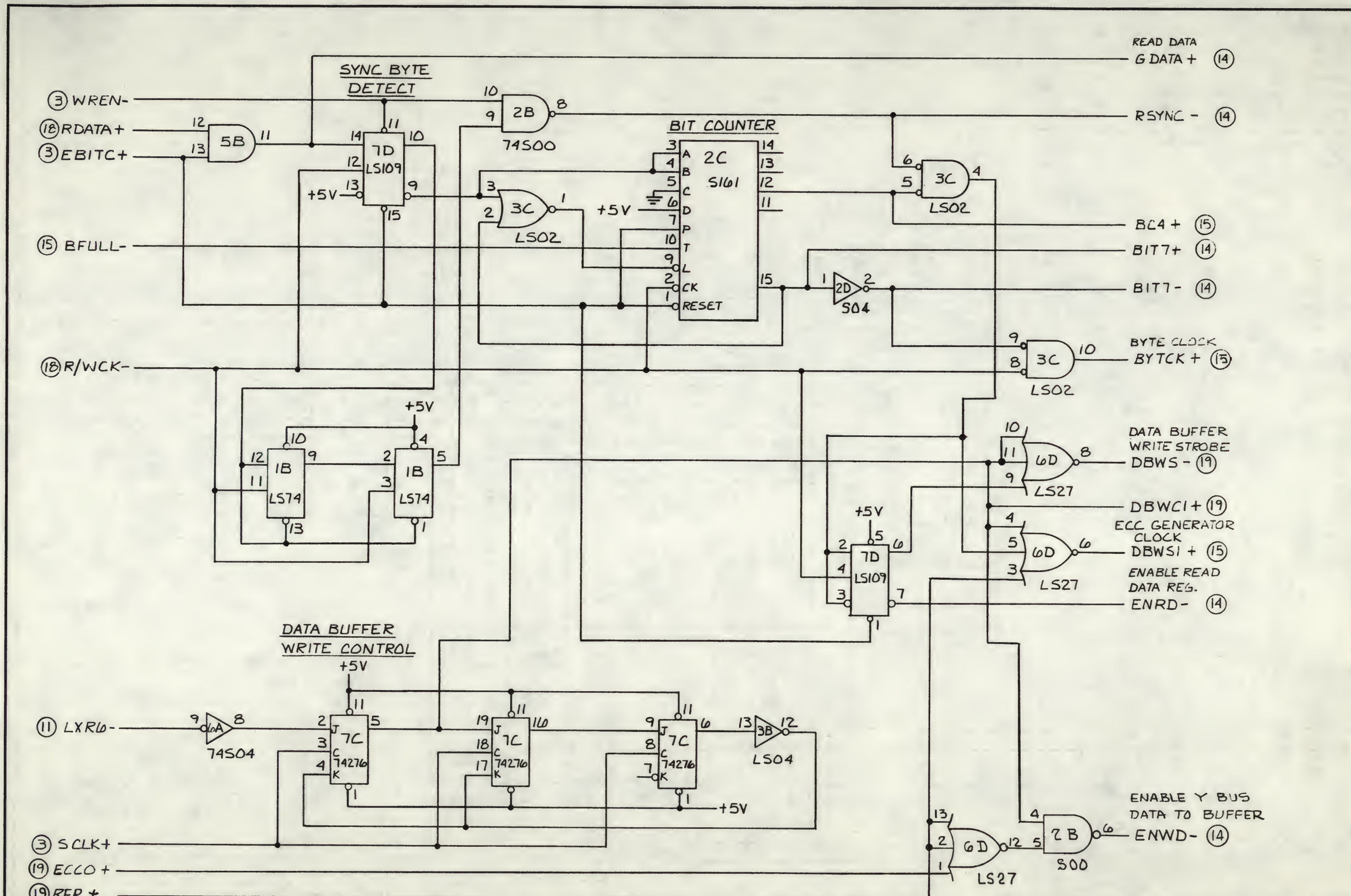
DISTRIBUTED LOGIC CORP.

SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM		SHT 11 OF 20
		DRAWING NUMBER 853027 B

17X22 PRINTED ON NO. 1000H-10 CLEARPRINT



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 12 OF 20
		DRAWING NUMBER 853027 A



DISTRIBUTED LOGIC CORP

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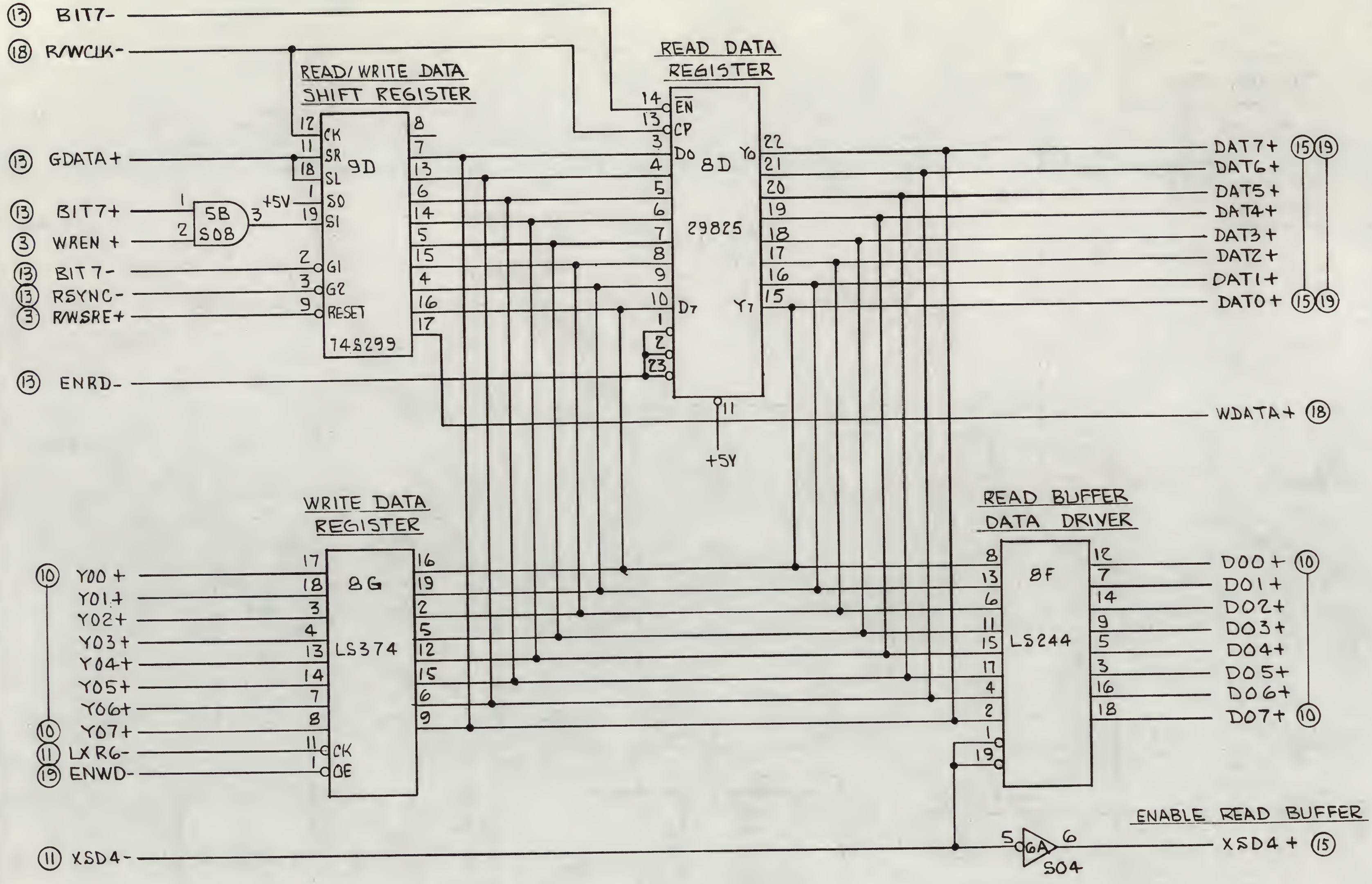
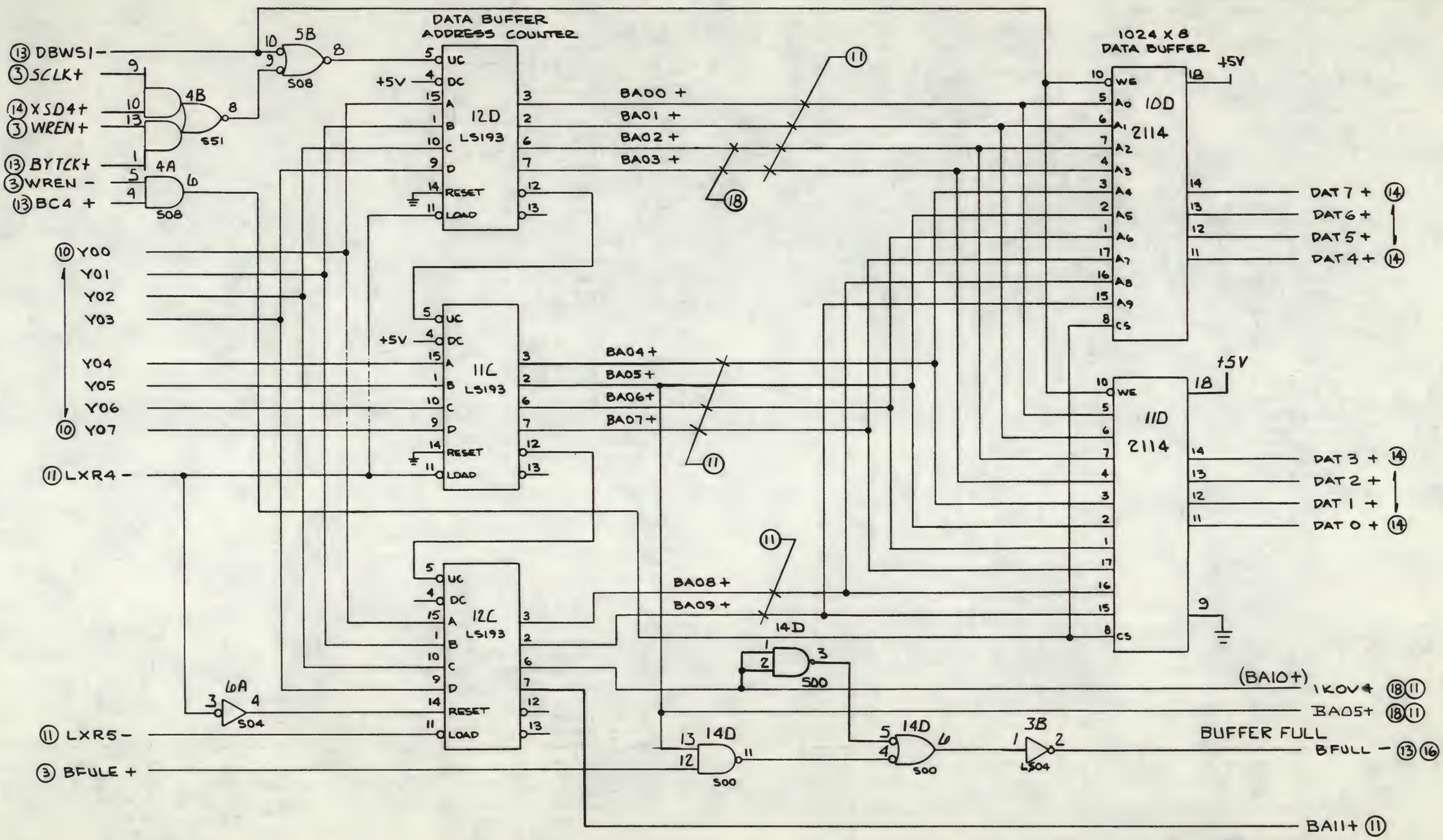
LOGIC DIAGRAM		SHT 13 OF 20
		DRAWING NUMBER 853027 D

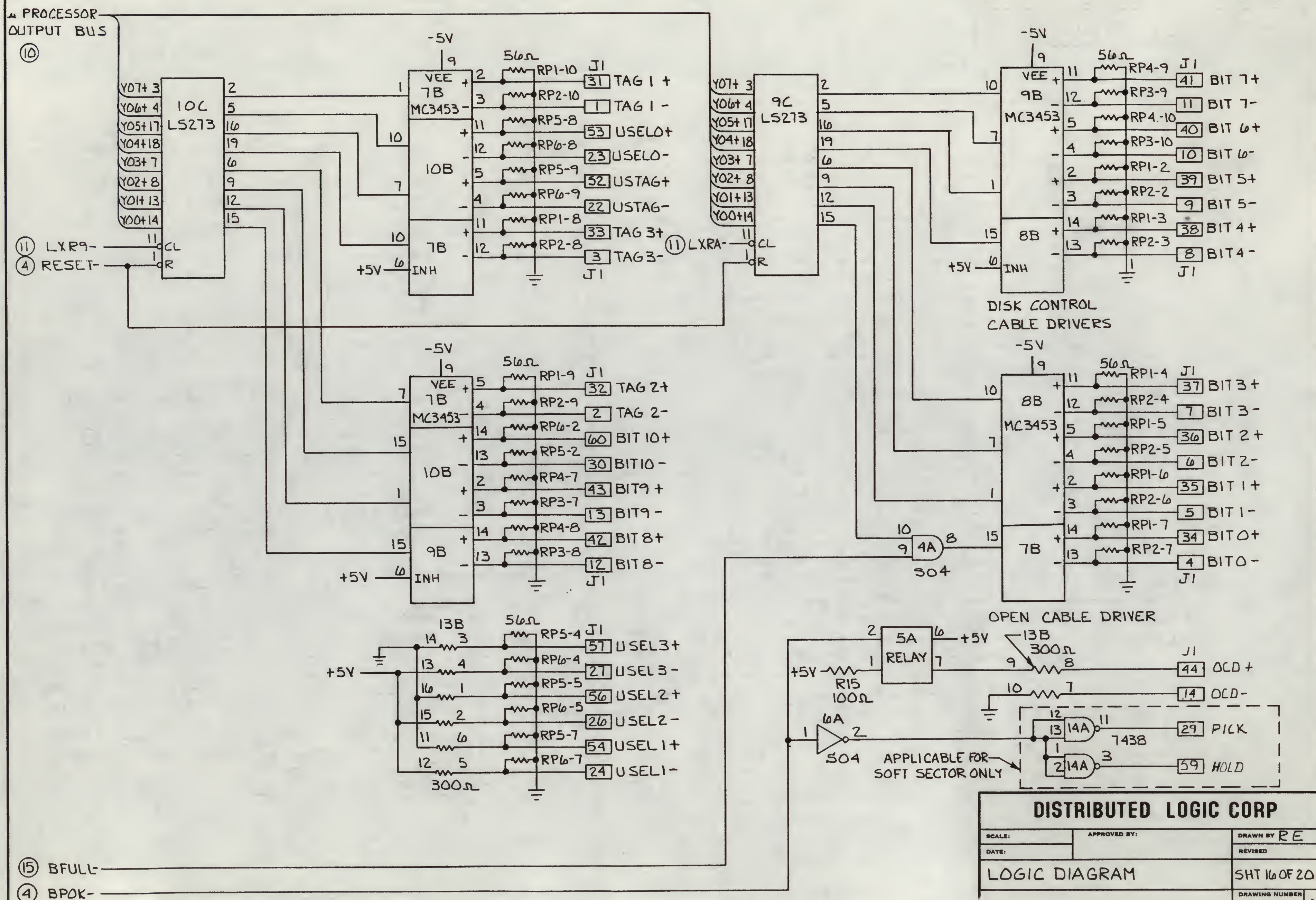


DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY
DATE:		REVISED
LOGIC DIAGRAM		SHT 14 OF 20
		DRAWING NUMBER 853027 C



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R. E.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 15 OF 20
		DRAWING NUMBER 853027 A

17X22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



DISTRIBUTED LOGIC CORP

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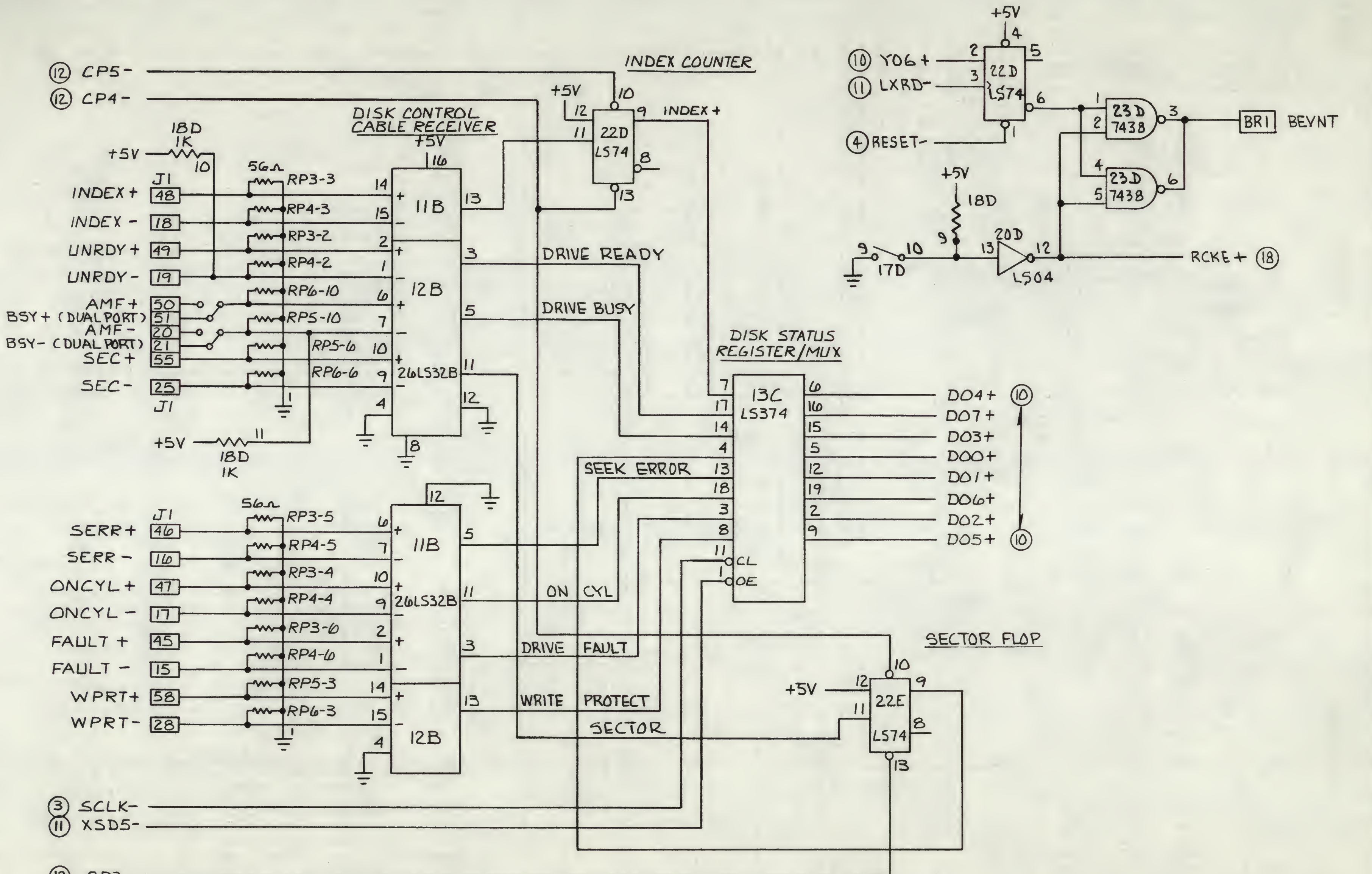
LOGIC DIAGRAM		SHT 16 OF 20
		DRAWING NUMBER 853027 A

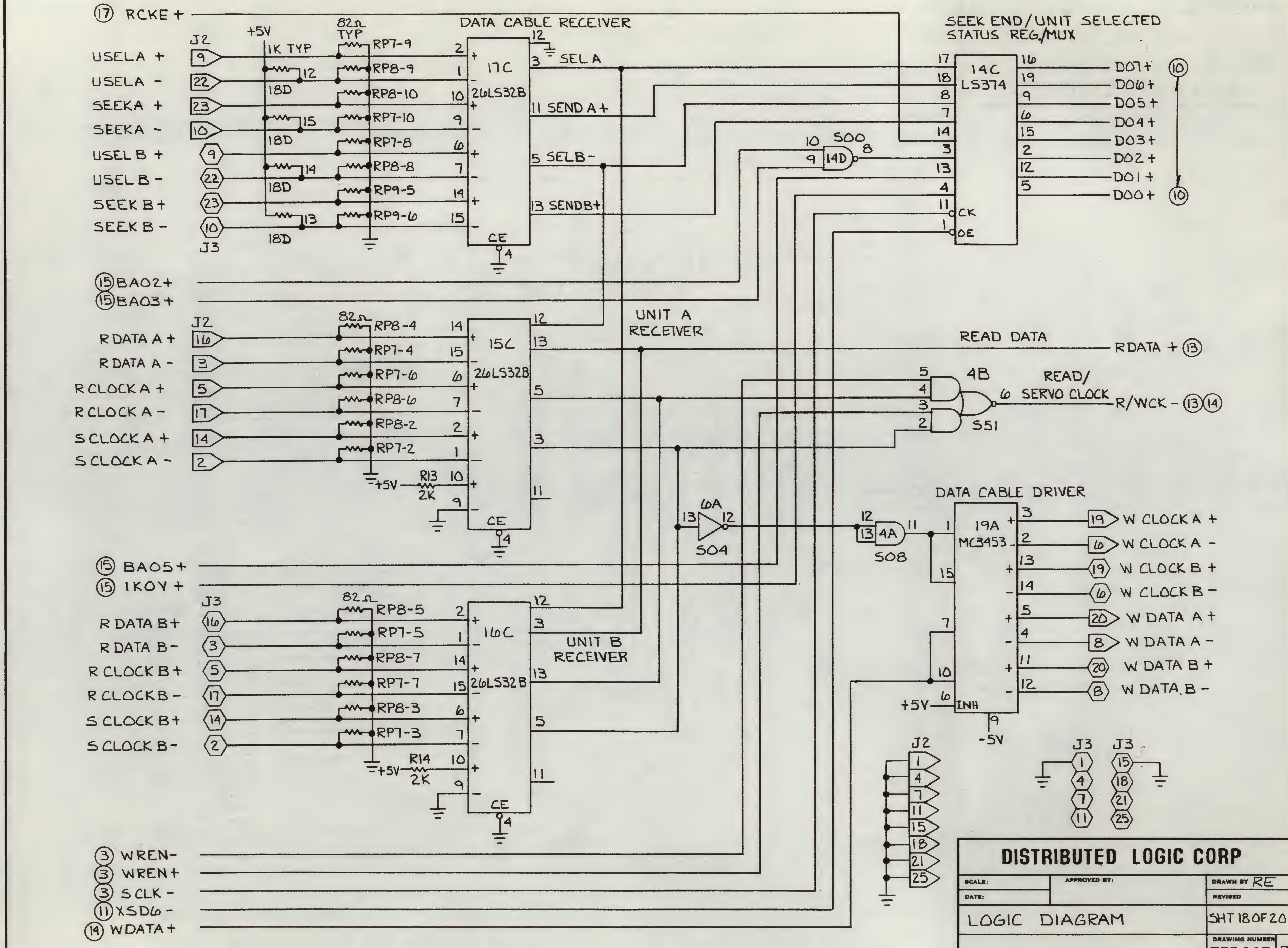
17 X 22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



DISTRIBUTED LOGIC CORP

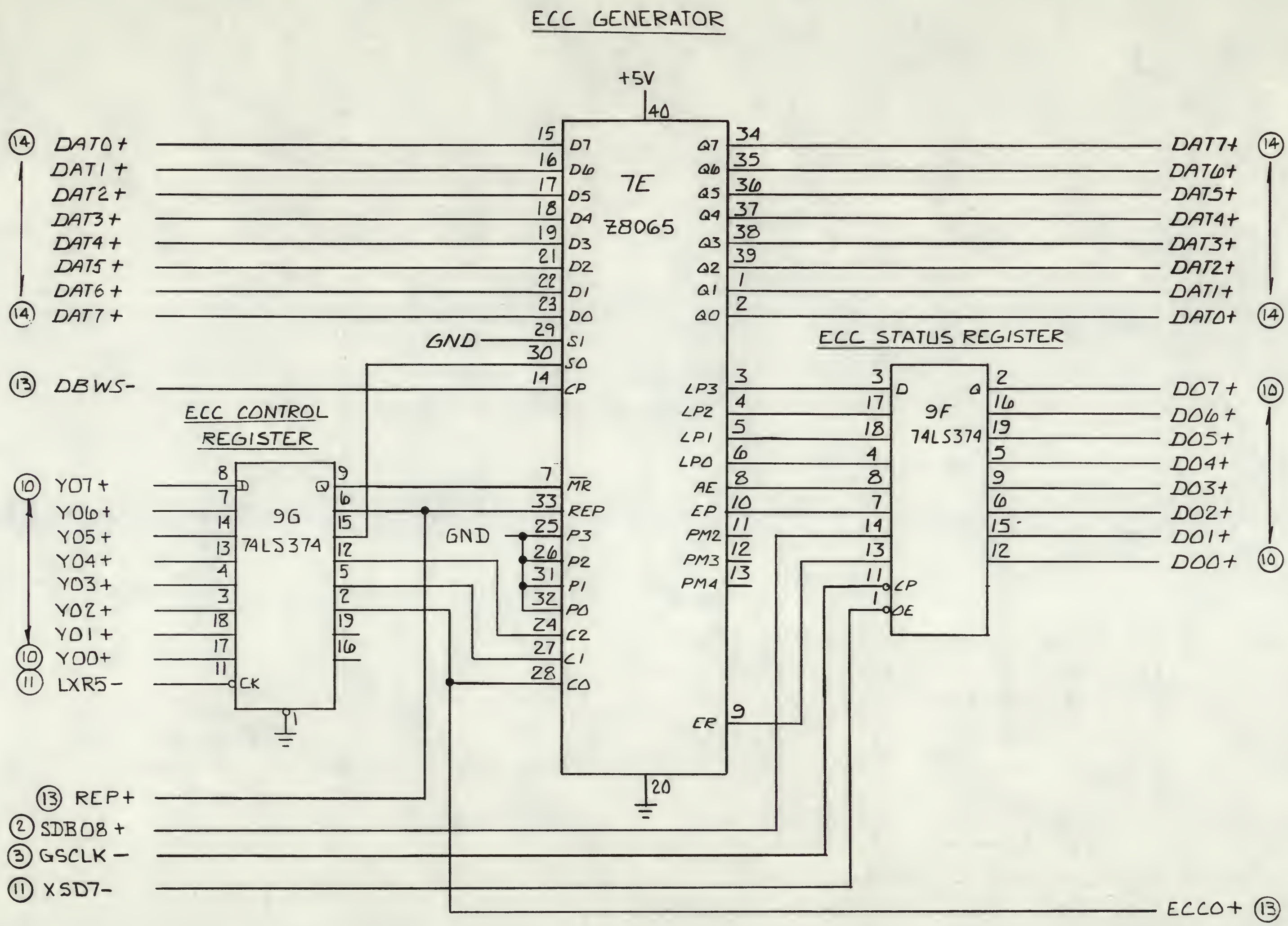
SCALE:	APPROVED BY:	DRAWN BY R E
DATE:		REVISED
LOGIC DIAGRAM		SHT 17 OF 20
		DRAWING NUMBER 853027 C

17 X 22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



DISTRIBUTED LOGIC CORP			
SCALE:	APPROVED BY:		DRAWN BY RE
DATE:			REVISED
LOGIC DIAGRAM			SHT 18 OF 20
			DRAWING NUMBER 853027 B

17 X 22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



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SCALE:	APPROVED BY:	DRAWN BY R. E.
DATE:		REVISED
LOGIC DIAGRAM		SHT 19 OF 20
		DRAWING NUMBER 853027 B

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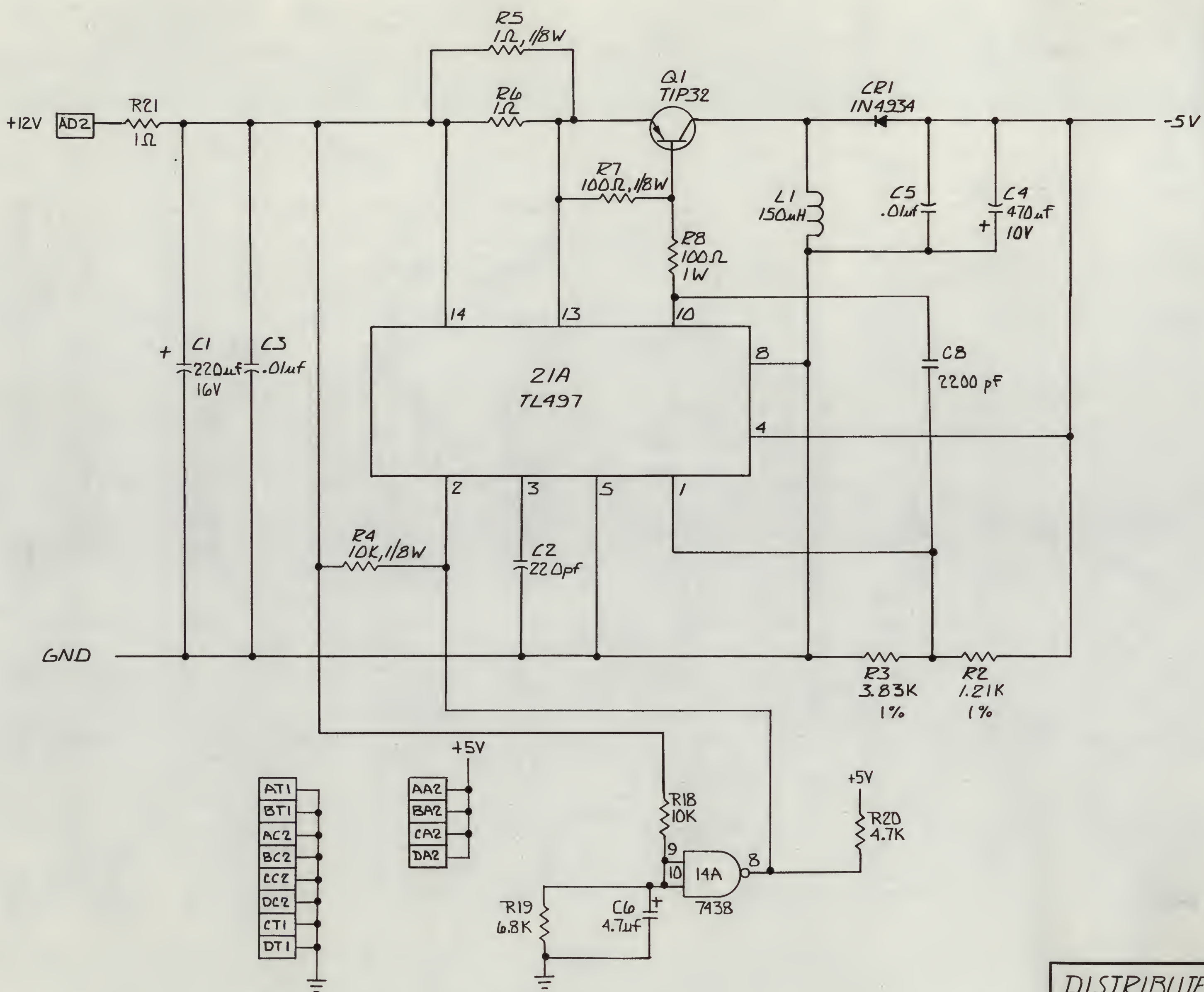
+12V TO -5V
POWER SUPPLY



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
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LOGIC DIAGRAM		SHT 20 OF 20
		DRAWING NUMBER 853027 B

17X22 PRINTED ON NO. 1000H-10 CLEARPRINT